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A Column-Parallel Hybrid ADC using SAR and Single-Slope with Error Correction for CMOS Image Sensors

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1. Introduction

Column-parallel ADCs using single-slope (SS) have been widely adopted in CMOS image sensors because they require simple column circuits with low power consumption [1][2]. However, very high clock frequency is used to increase operation speed since N-bit resolution requires 2^N clock cycles. On the other hand, column-parallel successive approximation register (SAR) ADCs provide fast conversion and low power consumption but occupy a large silicon area [3][4]. This is because they need a capacitor DAC (C-DAC) at column level with 2^N capacitors for N-bit resolution.

This paper presents column-parallel two-step ADCs using SAR and SS hybrid architecture to achieve fast conversion time and low power consumption without using high frequency clock and a large C-DAC. In addition, an error correction methodology is also proposed to compensate the variation of C-DAC for nonlinearity reduction.

2. Hybrid ADC Architecture

Fig. 1 shows a block diagram of the proposed column-parallel hybrid ADC. In a prototype design, an 11-bit ADC including a upper 6-bit SAR ADC and a lower 6-bit SS ADC with one redundancy bit is designed. The hybrid ADC achieves faster conversion than a 11-bit conventional SS ADC by using 6-bit SAR ADC. Comparing with the conventional SS ADC, it reduces the clock cycles to less than 1/ 2^5. Because of the reduction of clock cycles, the proposed ADC can perform at higher operation speed with lower clock frequency and thus can save power consumption. In addition, the required capacitors of a C-DAC are only 2^6 instead of 2^{11} for an 11-bit SAR ADC. Fig. 2 shows the hybrid ADC operation scheme and Fig. 3 depicts operation waveform. The SAR operation is first performed and then the SS operation is performed. The conversion time is 1.225 µs with 40 MHz clock frequency. A central ramp generator provides a 5.125-bit ramp signal with 32 + 4 voltage steps where 4 steps are for extended ramp counting. The extended counting avoids over-ranged residual voltage caused by cover range mismatch of the two-step ADC operation [5]. Furthermore, the hybrid architecture can also apply to a higher resolution than 11-bit.

Capacitor variation from C-DACs leads to nonlinearity and thus needs an error correction. A simple and effective error correction is very important, especially for actual commercial use. The proposed correction utilizes the generated ramp signal to calibrate the capacitor variation of all

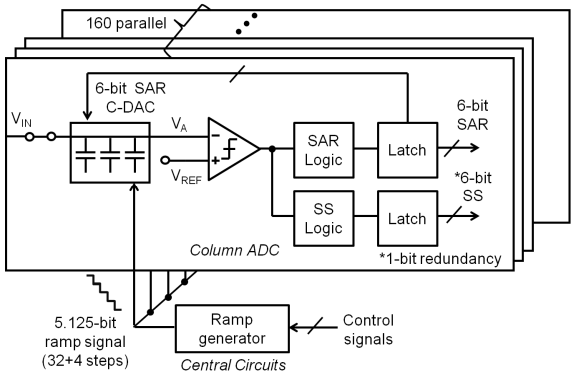

Fig. 1 Block diagram of proposed column-parallel hybrid ADC

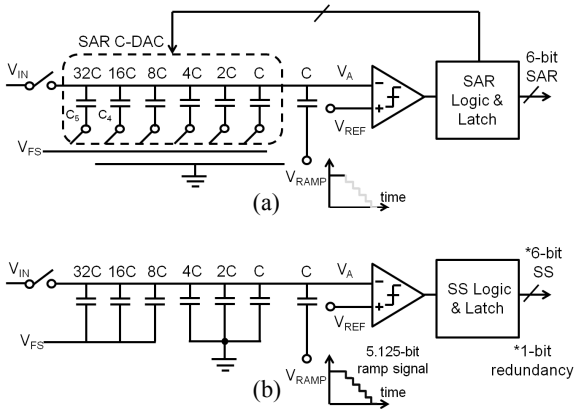

Fig. 2 (a) SAR operation scheme (b) SS operation scheme

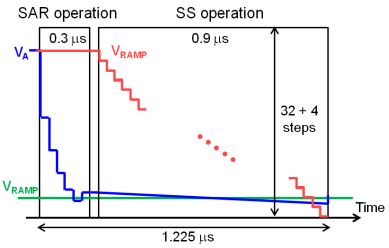

Fig. 3 Operation waveform

column C-DACs. Since a C-DAC is binary weighted, MSB capacitor value is ideally equal to the sum of other lower-weighted capacitors. In Fig. 4, it shows the error correction of the MSB capacitor (C_6). As shown in eq. (1), the MSB capacitor variation (ΔC_6) can be expressed by ΔV_{RAMP}. Initially, C_6 and C_5-C_0 are reset to low and high, respectively (Fig.4(a)). Next, C_6 is charged when ϕV_{in} turns off (Fig.4(b)). Subsequently, C_5-C_1 are discharged and then ramp signal starts to discharge C_0 for comparison (Fig.4(c)).

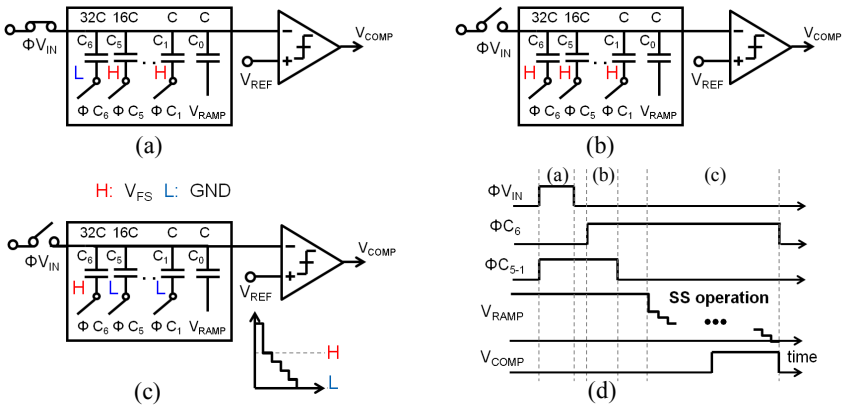

Fig. 4 Error correction of MSB capacitor (a) Reset capacitors (b) MSB capacitor charge (c) Discharge lower weighted capacitors and start ramp signal (d) Timing diagram

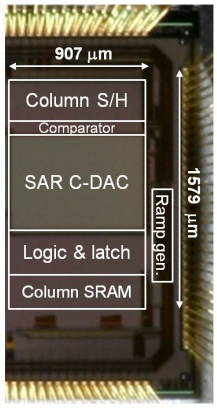

Fig. 5 Chip photograph

$$(C_6 + \Delta C_6)V_{FS} = \sum_{i=1}^{5} C_i V_{FS} + C_0 \Delta V_{RAMP} \quad (1)$$

Eventually, the error code of the MSB is acquired according to the comparison result (V_{COMP}). Fig.4(d) shows the timing diagram. The similar method is also used in the other lower-weighted capacitors of the C-DAC (C_5-C_1). After all error codes of the C-DAC are completed, digital post calibration is performed to compensate actual digital codes.

3. Results

The proposed ADC is fabricated in 0.18 µm 1P5M standard CMOS process. The hybrid ADC is composed of 160 column-parallel ADCs with 5.6 µm pitch. Fig. 5 shows the chip photograph. The column C-DAC is implemented by MIM capacitors with the unit capacitance of 24 fF. Fig. 6 shows the measured DNL and INL. Fig. 6(a) shows the measured results without extended counting and error correction. The DNL and the INL are +1.36/ -0.65 and +1.78/ -1.01, respectively. Fig. 6(b) shows the measured results with extended counting and error correction. After digital post calibration with error codes of C-DAC, the DNL and the INL are +0.40/ -0.44 and +1.21/ -1.12, respectively. A column ADC consumes 48 µW from separate 3.0 V and 1.2 V power supplies. TABLE I shows the measured summary.

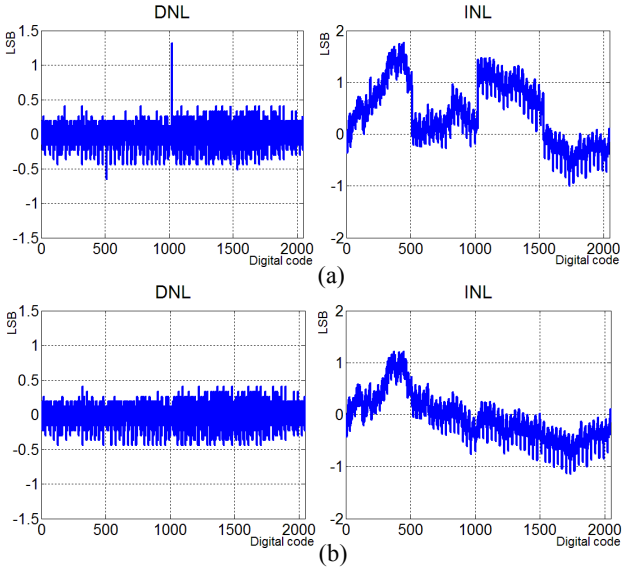

Fig. 6 DNL and INL (a) without error correction (b) with error correction

Table I Performance summary

Process	CMOS 0.18 µm 1P5M
Power supply	Analog 3.0V / Digital 1.2V
ADC resolution	11-bit
Input voltage range	1 Vpp
Maximum clock frequency	40 MHz
Minimum conversion time	1.225 µs
DNL (with error correction)	+0.40 / -0.44 LSB
INL (with error correction)	+1.21 / -1.12 LSB
Power consumption (1 column ADC)	48 µW

4. Conclusion

A hybrid ADC taking the advantages of SAR and SS architectures has been proposed. The 11-bit column-parallel ADCs achieve 1.225 µs conversion time with a clock frequency of 40 MHz and consumes 48 µW. In addition, the proposed error correction utilizes the SS central ramp signal to calibrate the column-level SAR nonlinearity without any additional circuit. The hybrid architecture provides good compromise between speed, silicon area, and power consumption. The proposed ADC architecture is suitable for high speed, small area, and low power CMOS imagers.

Acknowledgement

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