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A Programmable Difference-of-Gaussian Analog CMOS Image sensor Operating in the Subthreshold Regime

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1. Introduction

Image filtering is an important preliminary stage in many image processing algorithms. The computational image sensor is a promising solution since more transistors can be implemented for each pixel in advanced semiconductor fabrication technologies. For image filtering sensor, the programmability of the filter is a very important factor when adapting such an image sensor to various applications. However, many general purpose image sensors are limited to 3×3 kernel filtering scheme, and the kernel size can only be expanded by repeating these 3×3 kernel operations[1-2].

Among various kinds of filters, the Difference of Gaussian (DoG) filter is an indispensable processing employed in the well-known feature description algorithm named Scale-Invariant Feature Transform (SIFT) [3]. Moreover, it is well known in physiology that human retina can be seen as performing a retinal filter kernel [4], and that the retinal filter kernel has a center-surround organization, where its general model is a DoG. Therefore, DoG filter is important not only in general image processing but also in bio-inspired circuits.

To implement the DoG filter on the image sensor faces many challenges. One serious problem is the device variation, because it is rooted in the fundamentals of nature. Image sensors capable of compensating such process-variation-induced noises utilizing the floating-gate memory effect were reported [5]. However, this method needs large power supply and takes a few seconds during the process-variation cancelation, which severely limit the usage of this architecture.

In this paper, we present an analog CMOS image sensor architecture equipped with fully programmable Gaussian image smoothing filters and variable scale spatial DoG filters. They are both continuous functions and their kernel size is programmable according to the application need. In the design of a proof-of-concept chip, kernel size was made programmable from 3×3 up to 25×25. Fabrication-process-variations have been alleviated by employing a switched floating-gate MOS (SFMOS) circuitry [6]. The circuit simulation results obtained from a 25×25 pixel array and measurement results of the pixel circuit verified this concept.

2. Architecture

The organization of the image sensor is shown in Fig. 1. The core of the system is an array of pixel circuits. The X^2 generator and Y^2 generator produce voltages proportional to X^2 and Y^2. The shift registers are used for kernel scanning in X and Y directions in combination with the switch array. The region of filtering is also defined by the switch array which is controlled by the data in the shift register. By changing the length of (1, 1, ... , 1) data string, the kernel size can be arbitrarily altered. Since DoG profile is produced by subtracting a wide and short Gaussian function from a slender and tall Gaussian function, realizing programmable Gaussian function is quite essential.

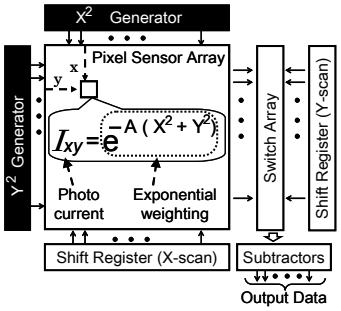

Fig. 1 Hardware organization of DoG analog CMOS image sensor.

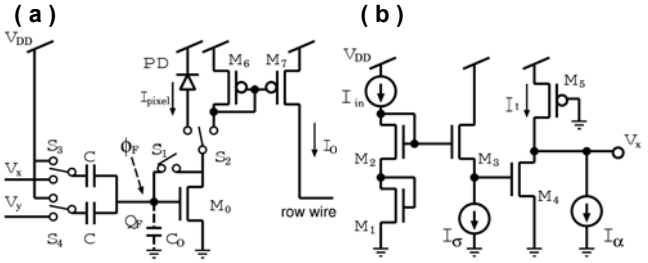

Fig. 2 Pixel circuit with an exponential weighting function (a) and Square-divider circuit (b).

A. Exponential Weighting Circuit

Fig. 2 (a) shows the pixel circuit having an exponential weighting function. A two-input SFMOS (vMOS) M_0 is used to memorize the photodiode (PD) current I_{pixel}. This circuit can cancel the process-variation error and, at the same time, multiply an exponential factor $e^{-A(Vx^2+Vy^2)}$. The circuit operates in two steps. In the first step, S_1 and S_2 are closed and M_0 memorizes I_{pixel} as a current memory. Then its gate voltage ϕ_F is determined according to the MOS subthreshold characteristics:

$$I_{pixel} = I_S e^{\beta\phi_F} \quad (1)$$

Here, $\beta = \frac{kT}{nq}$. At this moment, both S_3 and S_4 are connected to V_{DD}. Therefore, ϕ_F is determined as

$$\phi_F = \frac{2CV_{DD} + Q_F}{C_T}, \quad (2)$$

where $C_T = 2C + C_O$ and Q_F is the charge on C_O. Assuming $C_O << C$, Eq. (1) can be rewritten as

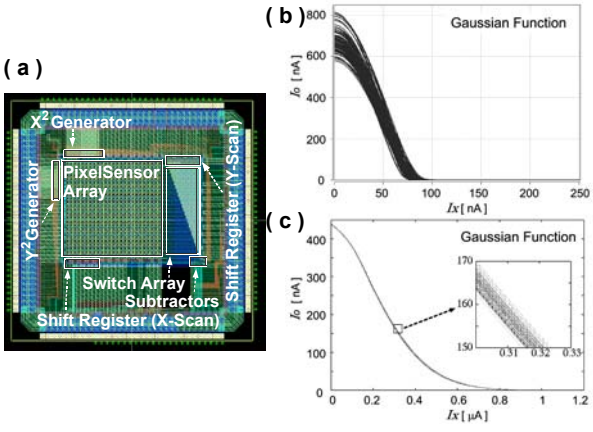

Fig. 3 Layout of the proof-of-concept composed of 25×25 pixel circuits (a). Monte Carlo simulation of Gaussian profile circuit without SFMOS (b) and with SFMOS (c)

$$I_{pixel} = I_S e^{\beta(\frac{Q_F}{C_T}+V_{DD})}. \quad (3)$$

In the second step, S_1 is opened and S_3 and S_4 are connected to V_x and V_y, respectively. Then the current flowing in M_0 changes to $I_{Gauss.}$, which is given by

$$I_{Gauss.} = I_S e^{\beta(\frac{Q_F}{C_T}+\frac{1}{2}(V_x+V_y))}. \quad (4)$$

Dividing Eq. (4) by Eq. (3), we obtain

$$I_{Gauss.} = I_{pixel} e^{\beta(\frac{1}{2}(V_x+V_y)-V_{DD})}. \quad (5)$$

It should be noted that I_S ($I_S \propto e^{-\beta V_{TH}}$), which mainly causes FPN, has disappeared in Eq. (5).

B. Square-Divider

X^2 generator in Fig. 1 is an array of square-divider circuits. Fig. 2(b) shows a square-divider circuit, which is composed of a squaring circuit based on the translinear principle (M_1, M_2, M_3, M_4) and a PMOS M_5 operating in the linear region.

$$V_x = V_{DD} - R I_t = V_{DD} - R(\frac{I_{in}^2}{I_\sigma} + I_\alpha), \quad (6)$$

where, R represents the equivalent resistance of the PMOS. The same circuits are used in Y^2 generator. Therefore, by setting $I_{in} = I_x$ in X^2 generator and $I_{in} = I_y$ in Y^2 generator, the current flowing in the pixel circuit locating at (x, y) is obtained from Eq. (5) as

$$I_{Gauss.} = I_{pixel}\, A\, e^{-\frac{\beta R}{2I_\sigma}(I_x+I_y)}. \quad (7)$$

Here $A = e^{-\beta R I_\alpha}$. The Gaussian kernel profile can be arbitrarily programmed by changing I_σ and I_α as parameters. A DoG filter is produced as the subtraction of two Gaussians of different shapes. Subtractors in Fig. 1 are used for this purpose.

3. Simulation and Measurement results

Fig. 3(a) shows the layout of the proof-of-concept chip and Monte Carlo simulation (V_{TH} fluctuates within the ±0.02V range) of Gaussian profile circuit without SFMOS (b) and with SFMOS (c), corresponding relative error is 20.27% and 2.1% respectively. Fig.4 shows the measured waveforms from Gaussian generator which verified the width of

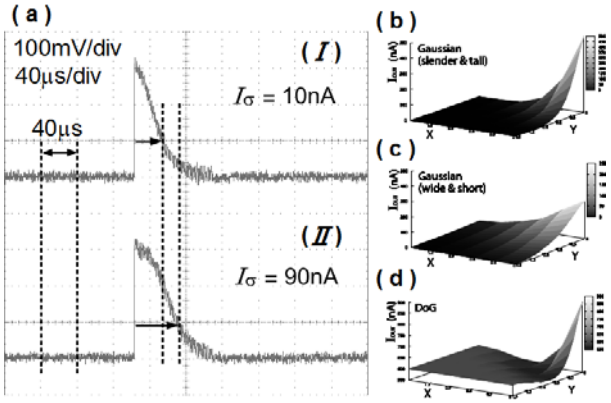

Fig. 4 Measured waveforms of Gaussian profile circuit (a) and two Gaussian kernel profiles (b)(c) and DoG kernel profile (d).

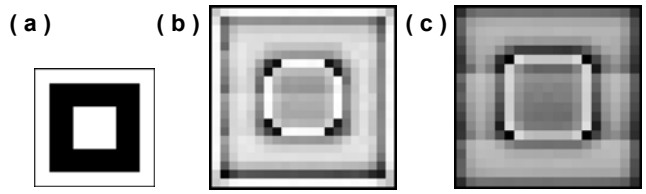

Fig. 5 Input image (a) and two filtered images of 5×5 (b) and 7×7 (c) kernels.

Table. I Comparisons with related work.

	This work	[5] (2007)
Technology	0.18-μm 1P5M CMOS	0.5-μm 2P3M CMOS
Die size (mm^2)	2.5 × 2.5	3 × 3
Pixel pitch (μm^2)	40 × 40	18 × 18
Fill factor (%)	35	13.4
Method	Switched floating-gate	Hot electron injection
Fixed-pattern noise	canceled	canceled
Filter name	Gaussian & DoG	No filter
Operation speed (fps)	≥ 300	8.7
Calibration time	5μs	4s
Power supply (V)	1.8	≥ 3.3

Gaussian profile is programmable. Two Gaussian kernel profiles and DoG profile obtained by HSPICE simulation are also shown in this figure as (b), (c), and (d). In Fig. 5, the HSPICE simulation results of 5×5 and 7×7 DoG filtering are illustrated as 2D maps (Darker color means a smaller value). Horizontal stripe lines are produced by the loss of changes in M_0 (Fig. 2(a)) due to transistor leakage during the kernel scanning. It shows the effect of parallel processing of every five and seven rows for 5×5 and 7×7 kernels, respectively. Characteristics of DoG filters are well observed. Comparison with related work in chip specifications and functional features are presented in Table I.

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