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Sensitivity of SRAM Operation against AC Power Supply Voltage Variation

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Abstract

False operation of SRAM cells is investigated under sinusoidal voltage variation on power lines. A standard SRAM core of 16k byte in a 90 nm 1.5 V technology is diagnosed with built-in self testing and on-die noise monitoring. The sensitivity of bit error rate is shown to be high against the frequency of variation while not much influenced by the difference in phase or in frequency against SRAM clocking. It is also observed that the distribution of fail bits becomes substantially random in a cell array with the higher frequency of disturbance.

1. Introduction

The stability of SRAM cells in safety-related VLSI systems, such as in automotive applications, is of critical importance. Those systems often encounter environmental disturbances like electromagnetic interference (EMI) and signal integrity (SI) problems. SRAM becomes dense with scaled devices for large capacity and operates under extremely low voltage for power saving. Dynamic stability of SRAMs has been addressed for SRAM cells specialized for micro processors in extremely low voltage operation [1][2]. In contrast, this paper focuses on false operation of SRAM cells under power supply voltage variation, in a traditional 6 transistor design that is generally used in ASICs.

2. Measurement system

The measurement system of Fig. 1 diagnoses the operation of an SRAM core with built-in self testing (BIST) and on-die noise monitoring (ODM), under the radio frequency (RF) voltage variation on power supply lines. Direct RF power injection (DPI), following to the immunity evaluation method of IEC 62132-4, is applied. The bit error rate (BER) and fail bit map (FBM) are evaluated by BIST. Dynamic voltage waveforms on power nodes of the SRAM cell array are captured by ODM to quantify voltage variation.

A test chip uses a 90 nm 1.5 V CMOS technology and embeds SRAM cores and the circuits for diagnosis. The SRAM core has three independent power domains for an SRAM cell array (V_{ddm}), peripheral circuits (V_{ddp}), and BIST function (V_{dd}). A single ground wiring network of V_{ssm} is shared with taps to a p-type silicon substrate. The details of measurement methodologies should be referred to [3][4].

3. Experimental results

The on-chip captured waveforms of power lines in SRAM cells under DPI are given in Fig. 2. SRAM operates at F_{clk} = 100 MHz. Power supply noise due to SRAM operation is synchronous to F_{clk} as observed on V_{ddp}, while superposed by the sinusoidal voltage variation on V_{ddm} at the DPI frequency of F_{rf} = 80 MHz. V_{ssm} is also capacitively coupled to F_{rf}.

The minimum RF power to cause BER of 7.6E-6, corresponding to a single-bit failure in average in the 16k byte SRAM core, is defined as $P_{net\_min\_dpi}$ under DPI and measured against F_{rf}, as in Fig. 3. The vertical axis shows forward power, P_{net}, measured by a power meter after a directional coupler. The minimum instantaneous voltage of V_{ddm} is derived as $V_{ddm\_min\_dpi}$ from the on-chip measured waveforms on V_{ddm} during DPI with RF power of $P_{net\_min\_dpi}$. The dependency of $P_{net\_min\_dpi}$ on F_{clk} is also given, where F_{rf} is fixed at 80 MHz. BER is very sensitive to F_{rf} regardless of F_{clk}, and becomes smaller for the higher F_{rf}.

The phase difference between F_{rf} and F_{clk} insignificantly impacts on BER, as given in Fig. 4. The noticeable exception is found at $F_{rf} = F_{clk}$. The slight increase of $P_{net\_min\_dpi}$ results in smaller BER than in the case of $F_{rf} \neq F_{clk}$, with the same power level of DPI.

The nature of SRAM BER is further investigated. When the fail bits are randomly distributed in the cell array and also appear randomly for iterative operations, we call them random fail bits. On the other hand, some of fail bits that are fixed at locations and appear in every operation are named fixed fail bits. The distribution of these fail bits is given in a snapshot of Fig. 5.

The ratio of random fail bits in 16k byte approaches to more than 95% when BER is of the order of 1E-2, in response to the increase of F_{rf} as well as F_{clk}, as in Fig. 6. In contrast, it was confirmed that the fixed fail bits occupied more than 50% for static noise margin measurements (F_{rf} = 0 Hz).

The susceptibility of SRAM cells to AC power supply voltage variation is dominated by random events of corrupting bi-stable states. The false operation is triggered by the instantaneous reduction of V_{ddm} voltage due to incoming noise (as shown in Fig. 3(a)), regardless of the internal timing to SRAM cell and peripheral circuits, as long as BER is reasonably small.

4. Conclusion

False operation of SRAM cells in a standard SRAM core is diagnosed by on-chip measurement technologies. The observed knowledge will work on the design guidelines of SRAMs for desensitization against power supply integrity (PSI) and electromagnetic immunity (EMI).

Acknowledgements

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References

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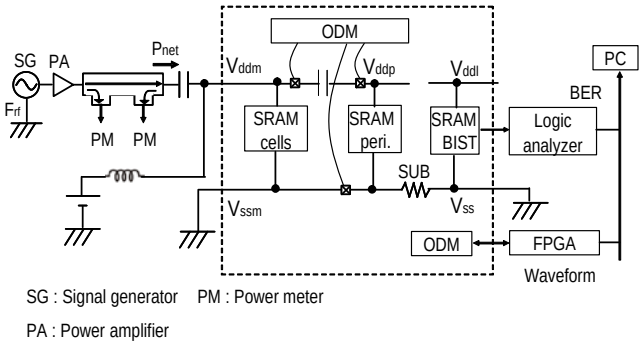

Fig. 1: Measurement setup for immunity evaluation using DPI and diagnosis by BIST and OCM.

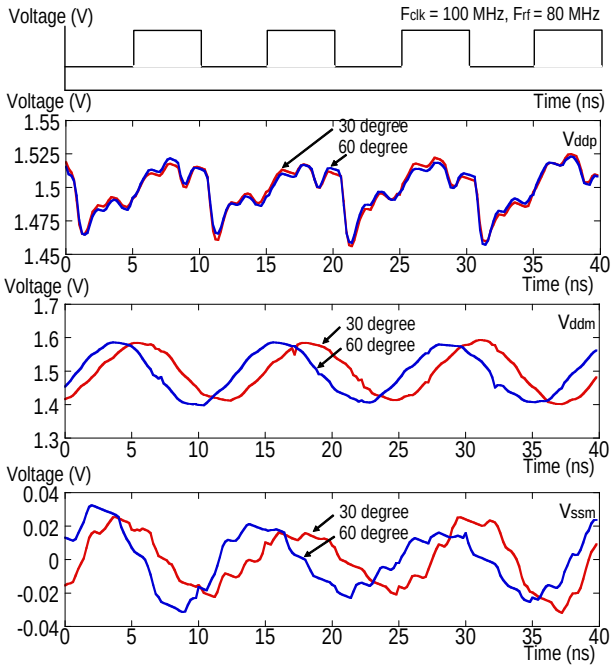

Fig. 2: Waveforms measured on power lines of SRAM cells under DPI. Phase difference of 30 degree and 60 degree.

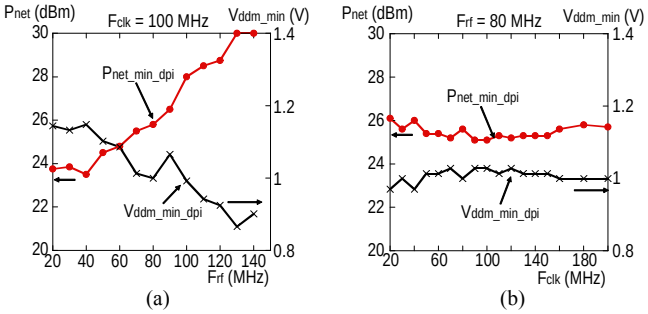

Fig. 3: (a) $P_{net\_min\_dpi}$ versus F_{rf}. (b) $P_{net\_min\_dpi}$ versus F_{clk}. $V_{ddm\_min\_dpi}$ is also shown.

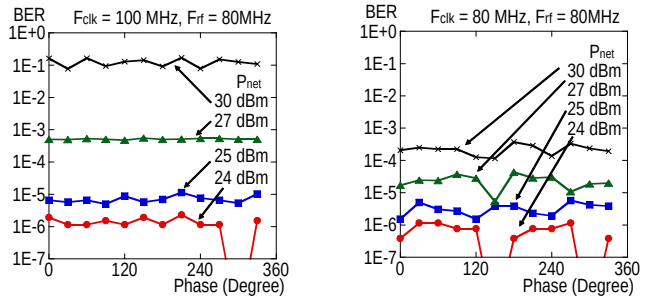

Fig. 4: BER versus phase difference with various P_{net}. (a) $F_{clk} \neq F_{rf}$, (b) $F_{clk} = F_{rf}$.

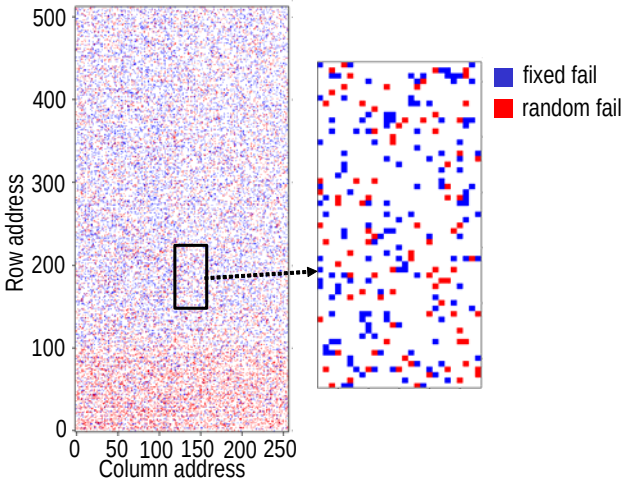

Fig. 5: Distribution of random and fixed fail bits in SRAM cell array.

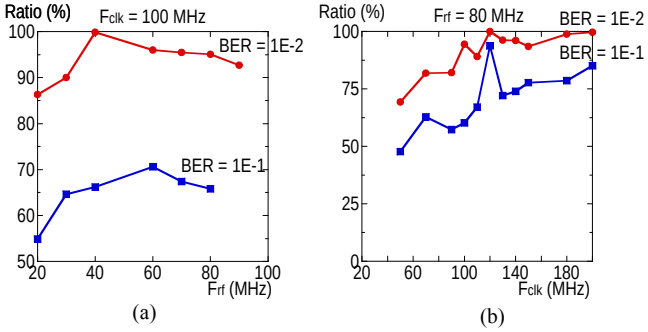

Fig. 6: Ratio of random fail bits in response to (a) F_{rf} and (b) F_{clk}.