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Variability Analysis of Sense Amplifier for Subthreshold Ultra-Thin-Body SOI SRAM Applications

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Abstract— ***This paper investigates the impact of variability on the robustness of subthreshold Ultra-Thin-Body SOI Sense Amplifier (UTB SOI SA) for SRAM applications. Specifically, intrinsic device variabilities due to gate Line Edge Roughness (gate LER), Work Function Variation (WFV) and Random Telegraph Noise (RTN) are included in our model library and used for the statistical analysis of subthreshold UTB SOI SA. Our results indicate that for Current Latch Sense Amplifier (CLSA), the offset voltage calculated solely from the threshold voltage (V_T) mismatch will underestimate the actual dispersion and the error will increase with decreasing V_{dd}. For large-signal inverter sensing, sense "0" will limit/dominate the overall sensing margin. In the presence of RTN, extra degradations in the sensing margin are observed and need to be considered.***

1. Introduction

UTB SOI MOSFET for subthreshold SRAM applications has been shown to exhibit advantages in cell stability and variability [1-2]. Fig. 1 illustrates the schematic of SRAM array in READ operation. In addition to the robustness of SRAM cell, the functionality of SA determines the correctness of sensing action and merits detailed investigation. In this paper, a model-assisted statistical approach [3] is carried out to efficiently consider multiple variation sources simultaneously and to evaluate the robustness of subthreshold UTB SOI SA. Our analysis is based on the UTB SOI MOSFET with L_{eff}=25nm, T_{ch}=5nm, T_{BOX}=10nm and EOT=0.65nm.

2. Operation of UTB SOI Sense Amplifier

Two commonly used sense amplifiers are evaluated: (1) small-signal differential sensing using Current Latch Sense Amplifier (CLSA, shown in Fig. 1 [4]) and (2) large-signal inverter sensing (Fig. 1). For CLSA in Fig. 2(a), Sense Enable (SE) signal is "Low" in Standby and pre-charges INT1/INT2 to "High" state. The high-going SE signal activates CLSA as BL/BLB differential voltage reaches the specified value that should be larger than the input offset voltage (V_{OS}, due to current mismatch between two branches) of CLSA [5]. For large-signal single-ended sensing, an inverter is employed to sense either BL or BLB signal (Fig. 2(b)). To ensure correct READ operation, robust SA design in the presence of possible variation sources is required. Similar to the approach in [1], we derive analytical V_{OS} and inverter trip voltage (V_{trip}) models that can be used to evaluate the robustness of SA. Fig. 3 shows the verification and accuracy of the proposed models to describe L_{eff} and Work Function (WF) dependencies. As can be seen, our models exhibit excellent accuracy with mixed-mode TCAD results for the cases studied.

3. Variability Analysis of Subthreshold UTB SOI Sense Amplifier

Fig. 4 shows the I_{ds}-V_{gs} dispersion of UTB SOI MOSFET using TCAD atomistic Monte Carlo simulations [6] accounting for gate LER [7] and WFV [8] at the same time. At V_{dd}=0.4V, satisfactory I_{ON}/I_{OFF} ratio (2×10^3X) is observed for the worst-case condition. Based on the simulated gate LER and WFV dispersions, the approach in [3] is applied to build model library for the variability analysis of subthreshold UTB SOI SA. For gate LER, we use a set of effective L_{eff} and effective WF to describe the subthreshold characteristics of individual device and the discrepancies between the calibrated model and TCAD simulations for each case are shown in Fig. 5(a). For the WFV-induced dispersion shown in Fig. 5(b), the observed Subthreshold Swing (S.S.) variation is negligible and Φ_m (or V_T) variation alone is employed to create the model library. Using the established model libraries, the influences of device variability on SA robustness are analyzed in Fig. 6 and Fig. 7. As can be seen, the proposed model-assisted approach shows fairly good agreement with TCAD simulations in describing V_{OS} and V_{trip} dispersions. Fig. 6(b) shows the comparisons of σV_{OS} between 3 different approaches at various V_{dd}. Due to the significant S.S. variation caused by gate LER, the model-assisted approach considering both gate LER and WFV exhibits larger V_{OS} variation and stronger V_{dd} dependence. Furthermore, opposite V_{dd} dependence is observed for the case of using V_T mismatch alone which also significantly underestimates σV_{OS}, especially at lower V_{dd}. In Fig. 7, V_{trip} variations (for Inverter) are assessed and compared with σV_{OS} (for CLSA). It can be seen that the inverter SA exhibits better robustness and variation immunity ($\sigma V_{trip} < \sigma V_{OS}$).

Similar to the framework in [9-10], the dispersion of Bit-line voltages during READ operation can be determined by the extreme SRAM cells with least/nominal/most "cell" READ and Standby leakage currents for the analysis of sensing margins. Fig. 8 demonstrates the extreme BL/BLB voltages with 16 and 512 cells per Bit-line with worst-case Bit-line data pattern where all un-selected cells have identical data that is opposite to the selected cell. Because of the adequate I_{ON}/I_{OFF} ratio in UTB SOI device (Fig. 4), the "high-held" BLB level stays close to V_{dd}, while the "low-going" BL voltage exhibits larger dispersion due to the READ current variation in the selected cell. Fig. 9 illustrates the determination of sense margin for differential CLSA at t=100 nsec. In order to correctly sense the signal, the values of BL/BLB differential voltage should be larger than the maximum of V_{OS} dispersion. Thus, the differential sensing scheme can afford up to 53 (i.e. 32) cells per Bit-line. For large-signal inverter sensing, sense "0" and "1" margins are defined as the difference between the BL/BLB level and inverter V_{trip}. To ensure sense "0" operation, the low-going BL voltage must be lower than the minimum of V_{trip} (Fig. 10). Similarly, for sense "1" margin (Fig. 11), the "high-held" BLB voltage should stay above the maximum of V_{trip}. It is observed that the worse sense "0" margin limits the affordable number of cells per Bit-line.

In addition to gate LER and WFV, the importance of RTN increases with scaling due to its inverse area dependence [11] and its impact on SA variability is examined in this section. Fig. 12 shows the dependence of RTN amplitude on the position of single trap near channel/gate insulator interface. Similar to the planar BULK MOSFET [12], the trap placed at the center region of the channel exhibits the largest impact (worst position) and is used for the worst-case analysis of UTB SOI SA. For large-signal inverter sensing, the trapping/de-trapping in each transistor forms 4 possible V_{trip} combinations and the resulting ΔV_{trip} is around 8 mV (Fig. 13(a)). In Fig. 13(b), the minimum V_{trip} combination is selected and combined with gate LER and WFV. In the existence of RTN, V_{trip} lowering is observed and sense "0" margin is degraded. Fig. 14(a) and Fig. 14(b) illustrate the possible V_{OS} of various trapping/de-trapping combinations induced by RTN for CLSA. It is observed that the transistors connected to BL/BLB (A2/A3) suffer the highest impact and the maximum V_{OS} (worst case) occurs for the A0 and A2 transistors in trapped state. For the worst-case combination (Fig. 14(c)), inclusion of RTN shifts the V_{OS} distribution to higher value and limits the sensing margin.

Acknowledgement

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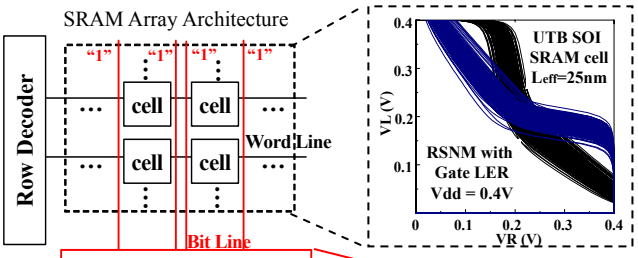


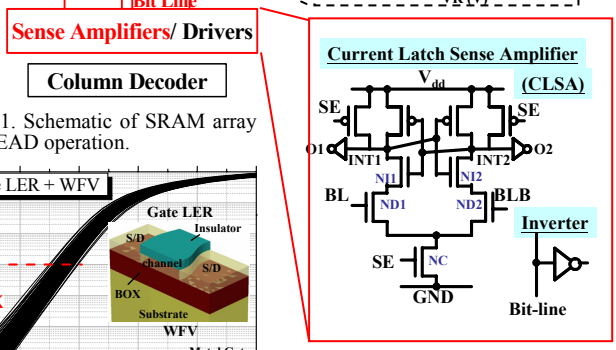


Fig. 1. Schematic of SRAM array in READ operation.

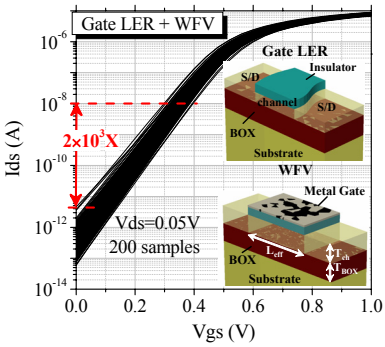


Fig. 4. The distribution of I_{ds}-V_{gs} characteristics of UTB SOI MOSFET considering gate LER and WFV.

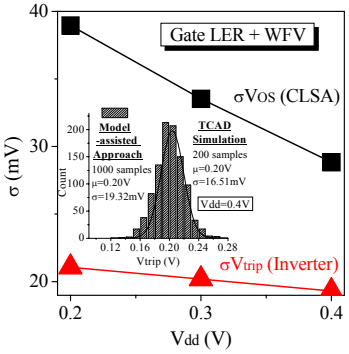


Fig. 7. Variability comparison of CLSA and inverter sense amplifier. The inset shows the V_{trip} comparison between TCAD simulation and model-assisted approach at V_{dd}=0.4V.

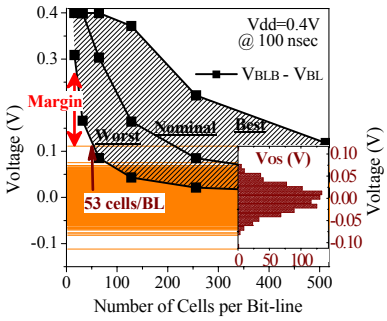


Fig. 9. Margin of differential CLSA at t=100 nsec. The values of Bit-line differential voltage should be larger than the maximum of V_{OS} dispersion (orange lines) to ensure correct sensing action.

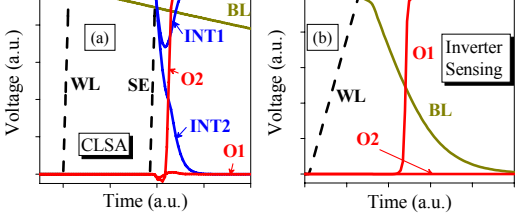


Fig. 2. The operations of sense amplifier for (a) small-signal differential sensing with CLSA and (b) large-signal sensing with inverter.

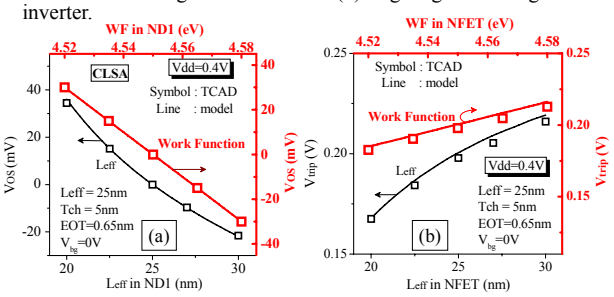


Fig. 3. Verification of (a) V_{OS} and (b) V_{trip} model for CLSA and inverter sense amplifier, respectively. The values of L_{eff} and Work Function (WF) are varied in ND1 (CLSA) and pull-down NFET (inverter) devices.

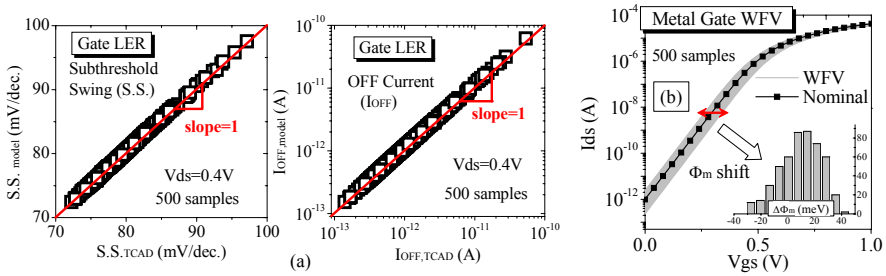


Fig. 5. Model calibration with atomistic TCAD simulations to build model libraries for gate LER and WFV. (a) The error analysis of S.S. and I_{OFF} for gate LER, and (b) determination of WFV library by Φ_m (V_T) shift.

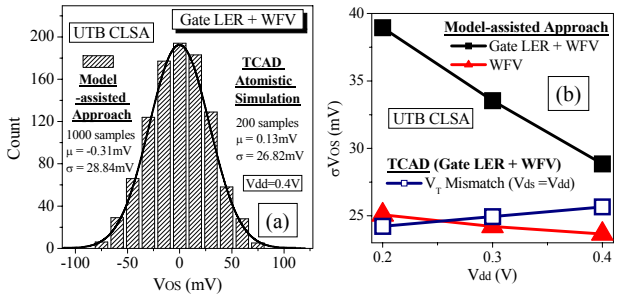


Fig. 6. (a) Comparison of V_{OS} variation between TCAD atomistic simulations and model-assisted approach considering gate LER and WFV and (b) the V_{OS} variation at various V_{dd}.

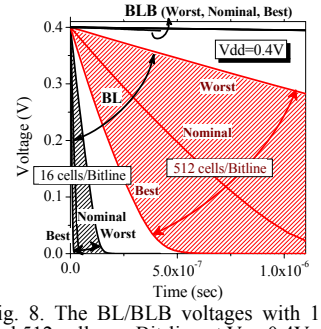


Fig. 8. The BL/BLB voltages with 16 and 512 cells per Bit-line at V_{dd}=0.4V.

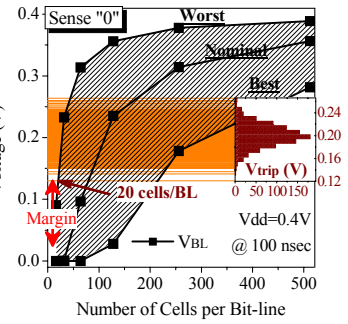


Fig. 10. Margin of large-signal inverter sense amplifier. The margin is defined by where all possible BL levels should be smaller than the minimum V_{trip}.

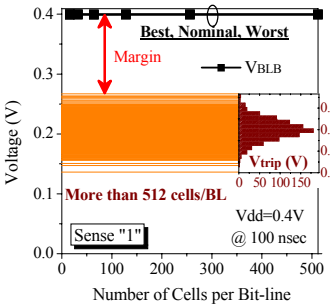


Fig. 11. Margin of large-signal inverter sense amplifier. The V_{trip} distribution should be lower than the possible BLB levels at the end of sensing action.

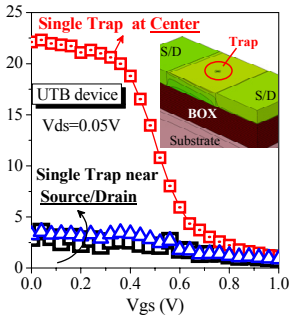
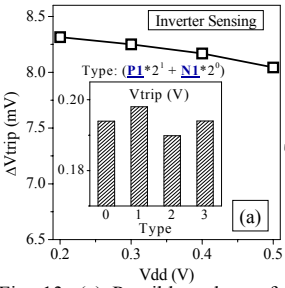


Fig. 12. Dependence of RTN amplitude on the position of trap at channel/gate insulator interface of UTB SOI device.



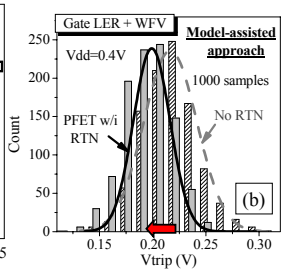
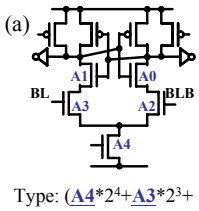
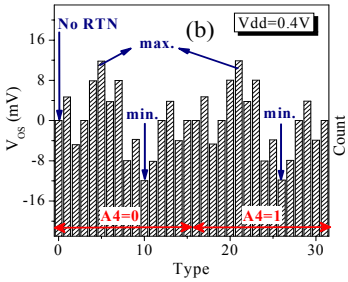


Fig. 13. (a) Possible values of inverter V_{trip} variation formed by trapping/de-trapping in each device and (b) the V_{trip} lowering due to RTN in the presence of gate LER/WFV. The bit value of "0" and "1" represent the "de-trapping" and "trapping" state, respectively.





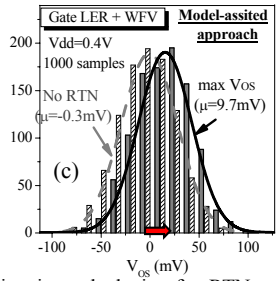


Fig. 14. (a) Binary-coded definition of trapping/de-trapping in each device for RTN analysis in CLSA and (b) the possible V_{OS} of various trapping/de-trapping combinations. (c) Comparison of V_{OS} distributions between the worst-case (max. V_{OS}) combination and the case without RTN.