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Ferroelectric synapse device with brain-like learning function: Analog conductance control in a ferroelectric-gate field-effect transistor based on the timing difference between two pulses

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1. Introduction

Neural networks, which are inspired from brain systems, consist of many neurons connected each other via synapses (Fig. 1 (a)). The synapses memorize the strength of the connection between pre- and post- neurons, called "synaptic weight". As a learning function, the synaptic weight is modulated to update the memorized information. In brains, their synaptic weights change depending on the relative timing difference between spike pulses of pre- and post-neurons, called STDP (Spike-Timing Dependent Plasticity), as shown in Fig. 1 (b) [1,2]. To realize the brain-like hardware neural networks, synapse devices with STDP function is needed.

We focus on an all-oxide ferroelectric-gate field-effect transistor (FeFET) as a candidate for the synapse device with a learning function [3-5]. The FeFET is a ZnO-channel FET using ferroelectric $Pb(Zr,Ti)O_3$ as a gate insulator. Owing to Coulomb interaction between electrons in the channel and the ferroelectric polarization, electrons are accumulated in the channel when the polarization is upward (Fig. 2 (a)). In contrast, electrons are depleted when the polarization is downward (Fig. 2 (b)). Accordingly, the channel conductance G can be modulated by the polarization, which is switched by applying the gate voltage V_{GS}. Note that the ferroelectric polarization remains after removing V_{GS}, which enables the nonvolatility of G. Figure 2 (c) shows the measured $G - V_{GS}$ characteristic, in which a counterclockwise hysteresis loop is observed, indicating G is dominated by the ferroelectric polarization switching. By using pulse voltage as V_{GS}, it is also possible to obtain an analog-like modulation of G. Figure 2 (d) shows the conductance measured before (G_{init}) and after (G_{pulse}) applying pulse gate voltage with various pulse heights V_{GS}^{pulse} (see an inset of Fig. 2 (d)). Utilizing these properties, a synaptic weight can be memorized in an FeFET as G [5].

In this work, we realized an FeFET-based synapse device with an STDP-based learning function. The real-time learning was also demonstrated for the first time.

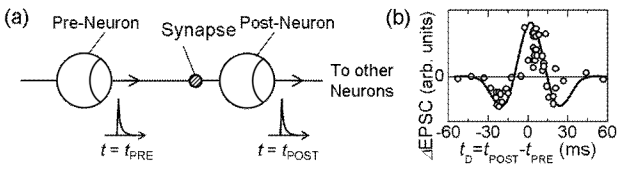

Fig. 1 (a) A schematic of neurons (pre- and post-) connecting via a synapse. (b) The measured change in excitatory postsynaptic current (EPSC) of a hippocampal neuron of a rat [2], which corresponds to the change of synaptic weight.

2. Synapse and neuron circuit

We propose a circuit comprising a synapse and a neuron (Fig. 3 (a)). The voltage signals of V_{PRE1} from the pre-neuron and V_{POST} from the post-neuron are used to update the synaptic weight, which is memorized as G. V_{PRE2} determines whether the signal from the pre-neuron is transmitted to the post-neuron. In learning, V_{PRE1}, V_{PRE2}, and V_{POST} are input to the synapse. The bipolar pulse V_{PRE1} is input to the gate of the FeFET via a selector which acts as follows. Only while V_{POST} is input, V_{PRE1} is given to the gate via the selector. While V_{POST} is not input, the selector keeps the gate grounded. Therefore the height of the pulse voltage V_{GS} applied to the gate depends on the relative input timing difference t_D of V_{PRE1} and V_{POST}. Considering the characteristic of the pulse voltage modulation of G plotted in Fig. 2 (d), the changes of G by applying V_{GS} depend on t_D, which corresponds to the STDP-learning. Unless the learning is performed, V_{PRE1} and V_{PRE2} are input and V_{POST} is not input to the synapse. As a result, V_{PRE1} does not modulate G. On the other hand, the signal transmission from the pre-neuron to the post-neuron is dominated by V_{PRE2}. V_{PRE2} turns on the switching transistor, and then the pulse current flows into the neuron. Note that the amplitude of the current is determined by G, meaning that the signal from the pre-neuron is weighted by the synapse. The input current is temporally integrated as an output voltage V_{OUT}

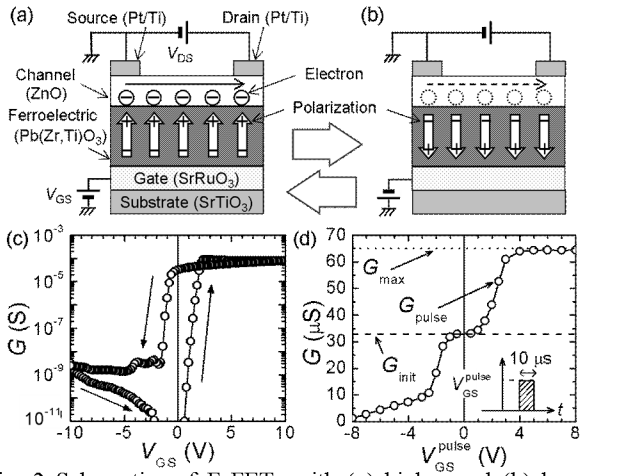

Fig. 2 Schematics of FeFETs with (a) higher and (b) lower conductance. (c) Gate voltage V_{GS} dependence on the conductance G of the FeFET. (d) G before (G_{init}) and after (G_{pulse}) applying a square-pulse gate voltage depicted in the inset with varying the pulse height V_{GS}^{pulse}.

by an analog integrator in the neuron. Accordingly, the updated G is reflected in the variation of V_{OUT}. When V_{OUT} exceeds a threshold voltage V_{th}, a waveform generator outputs two pulses to other neurons simultaneously. Then, one of the two pulses is given to the synapse as V_{POST}.

Owing to the three-terminal structure of the FeFET, the updating of the synaptic weight can be performed by just applying V_{POST} without canceling signal transmission among neurons, which is the same as brain systems, while the neural networks using the previously reported two-terminal synapse need to stop signal transmission for learning [6].

3. Spike-timing learning

A circuit with our own FeFET shown in Fig. 3 (a) was fabricated on a breadboard, and then we demonstrated an STDP-based learning in the circuit. Figures 3 (b)-(d) show the observed behavior of the selector in the case of t_D = -6, 0, 10, and 20 μs. Here, t_D is defined as the time difference between the centers of $V_{PRE1(2)}$ and V_{POST} depicted by arrows in Fig. 3 (b). V_{GS} changes depending on t_D as shown in Fig. 3 (d). Since V_{POST} decides whether V_{PRE1} is input to the gate or not, changes of the conductance ΔG before and after applying V_{PRE1} and V_{POST} were measured with varying t_D (Fig. 3 (e)). This result indicates that we successfully achieved STDP function because the $\Delta G - t_D$ curve resembles the biologically measured STDP (Fig. 1 (b)).

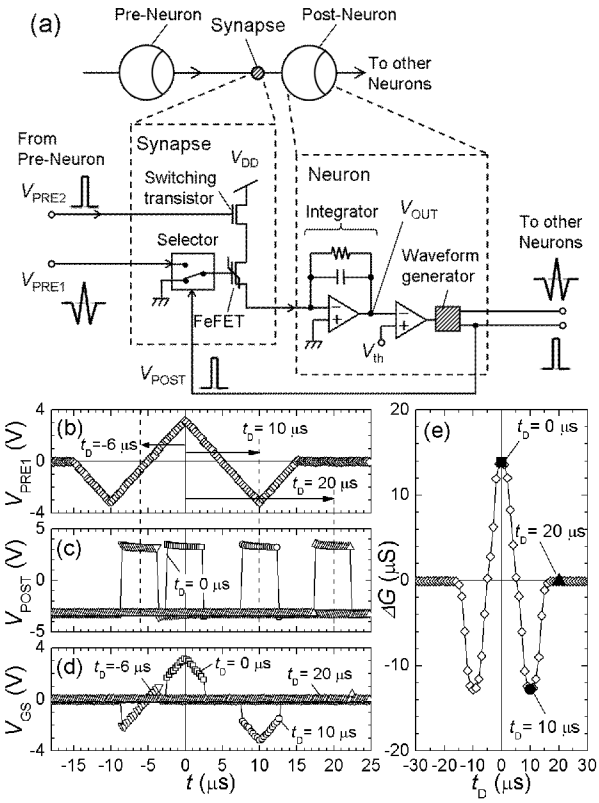

Fig. 3 (a) Schematics of a circuit with a synapse and a neuron. Time-sequence diagrams of (b) V_{PRE1}, (c) V_{POST}, and (d) the output of the selector V_{GS}, with different timing difference t_D of V_{PRE1} and V_{POST}. (e) Changes of the conductance of the FeFET ΔG by applying V_{PRE1} and V_{POST} with changing t_D.

Figures 4 (a)-(c) show two inputs V_{POST}, V_{PRE2} and output of the integrator V_{OUT}, respectively. The amplitude of V_{OUT} is increased during the input of V_{PRE2}, and then V_{OUT} decays after V_{PRE2} turns off the switching transistor with reflecting the leaky integration behavior. Around t = 0 μs, the STDP-learning was performed by applying V_{PRE1}, V_{PRE2} and V_{POST} with t_D = 0, 10, and 20 μs. In case of t_D = 0 μs, as the conductance becomes larger than that before learning (t < 0 μs), the peak heights of V_{OUT} also become larger than those at t < 0 μs. Adversely, the peak heights at t_D = 10 μs become smaller. However, at t_D = 20 μs, the peak heights did not change. These changes in V_{OUT} by the STDP-learning are consistent with the STDP property of FeFET shown in Fig. 3 (e). As above, the real-time signal transmission and the STDP-learning were successfully observed, which is necessary for the practical applications.

Utilizing the neuron circuit, it would be possible to realize an associative memory operation in a spike-based Hopfield-type feedback neural network [7] with STDP -based learning.

4. Conclusions

We demonstrated an STDP-based learning function in the synapse device composed of an FeFET, and successfully observed that in real-time the learning result was reflected in the behavior of a neuron for the first time. These results indicate the potential for realizing neural networks emulating behaviors of brain synapses.

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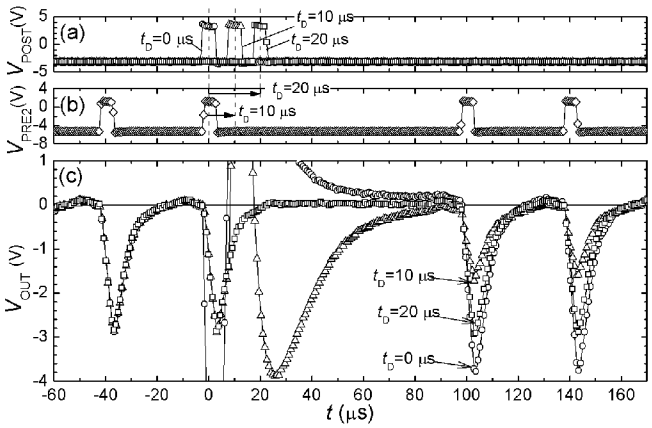

Fig. 4 Real-time measurements of (a) V_{POST}, (b) V_{PRE2}, and (c) V_{OUT} with changing the timing difference t_D between V_{POST} and V_{PRE2}.