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102.4 GS/s Impulse Sampling Circuit with Low Power and Low Timing Error Clock Generation

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1. Introduction

Ultra-wideband (UWB) systems have been applied to breast cancer imaging systems [1-2]. An equivalent time sampling method has been developed for low-power imaging system [3]. In the case of time-domain imaging systems, sampling rate of analog-to-digital converters (ADCs) is an important factor to improve the accuracy of reconstructed images [4]. The sampling rate is determined by the phase resolution of clock generation circuits [5, 6]. For realizing a 100 GS/s equivalent time sampling system, the PLL based 10 ps phase-resolution clock generation circuit is necessary.

In this paper, we have developed an impulse sampling circuit with low power consumption and high sampling rate with an improved clock generation scheme.

2. Clock generation scheme

A clock generation circuit shown in Fig. 1 has been developed for an UWB equivalent-time sampling system. A sampling clock should be synchronized with an input signal and the phase should be sequentially changed with a fine resolution (ΔT). The inverse of ΔT is equal to the sampling rate. The proposed circuits, which consist of a 16-phase output phase locked loop (PLL), a phase interpolator, a 64-to-1 multiplexer (MUX), a 16-to-1 frequency divider (DIV) and an 11-bit counter, are synchronized with the reference clock of PLL. The PLL is operated with the reference clock and generates the output of 1.6 GHz 16-phase differential clocks (the interval is 39.06 ps). To generate fine-phase clocks, the 16-phase clock signal is converted to 64-phase clocks using 2-stage phase interpolator. The clocks are selected by the MUX and the frequency is divided by 16. The DIV separates 10 ns period of input signal to make 16 sub-frames. The MUX makes the sampling point by 9.77 ps in the 625 ps sub-frame. As shown in Fig. 2, the 10 ns periodic-signal can be sampled by 1024 points using the 100 MHz shifting clock generated by the equivalent time sampling method. As a result, a 102.4 GS/s sampling rate can be achieved and the time axis of output signal is expanded. A 10 ns periodic input signal is converted to 32.768 μs. The ratio is 32768 which is equal to 2^{15}.

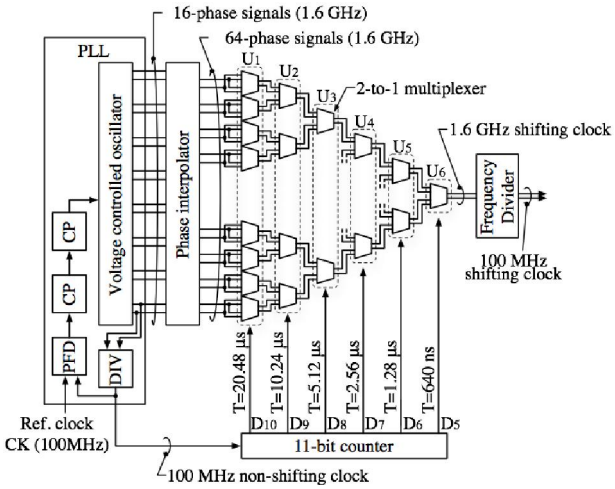

Fig. 1. Proposed clock generator.

3. Designing clock generation circuit

Phase interpolator

The phase interpolator consists of 2 stages as shown in Fig. 3. Each stage doubles the number of phase. The interpolated signals are generated by mixing the 2 closest-phase input signals using inverters. The resistors, which are connected to output node of inverters, are used for equalizing the output phases.

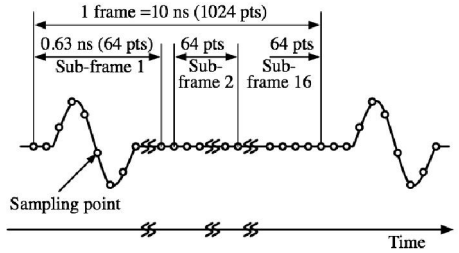

Fig. 2. Sampling points of 10 ns periodic signal.

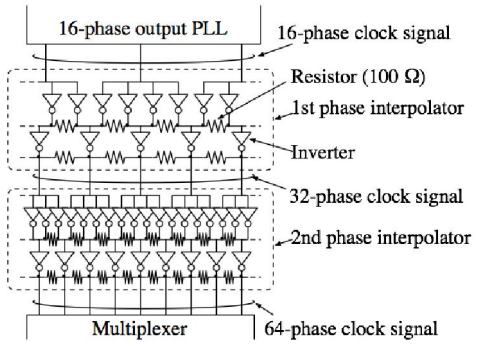

Fig. 3. Schematic of phase interpolator.

The simulation result of the phase interpolator is shown in Fig. 4. The phase delay between 2 closest signals is in 15.3 ps range (4.4 - 19.7 ps) without resistors. By inserting the resistors as shown in Fig. 3, the range of the phase delay decreased to 5.8 ps (7.3 - 13.1 ps). On the other hand, the power consumption increased as shown in Fig. 4(b). 100 Ω resistors are selected for phase interpolation. The performance comparison between PLL-based multi-phase clock generators is shown in Table I. Among the circuits, the proposed circuit achieves the smallest phase resolution with reasonable power efficiency.

64-to1 multiplexer

The 64-to-1 MUX consists of 63 2-to-1 MUX. Using the current mode logic type 2-to-1 MUX which is conventionally used for high-speed MUX, the output signal is degraded because of the interference of unselected signals. To prevent the effect, the switched cascade topology [3] is implemented in the proposed circuit. The simulation result of multiplexer is shown in Fig. 5. By using the switched cascade topology, the phase error is improved to 6.3 ps.

4. Measurement Results

A high speed sampling circuit was fabricated using 65 nm CMOS technology. The circuit consists of a track and hold circuit with resistive-feedback UWB matching circuit (Fig. 6(a)), a 4-bit A-D converter (Fig. 6(b)) and the proposed clock generation circuit. The die photograph is shown in Fig. 7. The supply voltage and the power consumption are 1.4 V and 125 mW, respectively. The measurement results of UWB signal are shown in Fig. 8. The horizontal axes of output signal are aligned to input signal. The UWB input signal which has 5 GHz center frequency is given as an input signal. By use of the shifting clock, the input signal was sampled with 102.4 GS/s sampling rate.

5. Conclusions

A 125 mW 102.4 GS/s ultra-high-speed ADC for an equivalent-time UWB system was developed using a 5.8 ps phase-interpolator and a switched cascade multiplexer. The phase interpolator achieved 9.8 ps minimum phase resolution with 0.3 mW/GHz/phase energy efficiency.

Acknowledgements

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References

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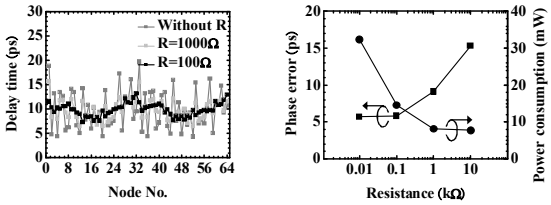


(a) (b)

Fig. 4. Simulation results of phase interpolator. (a) Delay time. (b) Phase error and power consumption.

Table I Performance Comparison of PLL-based Multiphase Clock Generator.

	[7]	[8]	[9]	This work
Technology	130nm	65nm	65nm	65nm
Supply voltage	1.2 V	1.2 V	1.0-1.2	1.4 V
frequency range	0.11-1.4 GHz	26-412 MHz	8 GHz	1.6 GHz
# of phase	40	63	4	64
Resolution	17.86 ps	38.5ps	31.25ps	9.8ps
Power consumption	77.4 mW	3.47 mW	21 mW	30.9 mW
Power effeciency (mW/GHz/phase)	1.38	0.13	0.66	0.30

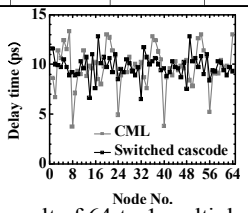
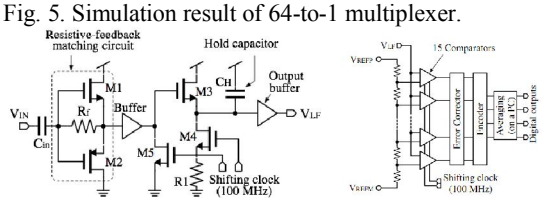


Fig. 5. Simulation result of 64-to-1 multiplexer.



(a) (b)

Fig. 6. Components of sampling circuit. (a) Track and hold circuit. (b) 4-bit flash ADC.

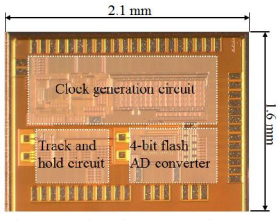
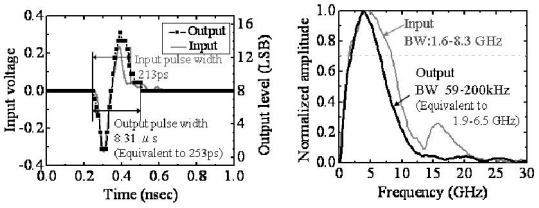


Fig. 7. Die photograph.

Table II Performance of Sampling Circuit

Technology	65 nm CMOS
Supply voltage	1.4 V
Sampling rate	100 GS/s
# of bit	4
Power consumption	125 mW
Chip size	2.1 mm x 1.6 mm



(a) (b)

Fig. 8. Measurement result with UWB input. (a) Waveforms. (b) Spectrums.