A DRAM Sense Amplifier Circuit by Multi-pillar Vertical MOSFET Realizing Sub-1V Core Voltage Operation without Overdrive Technique

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1. Introduction

Recently, reducing power consumption of DRAMs such as mobile DRAM has become increasingly important. From this aspect, a low core voltage (VCORE) in DRAM is needed; however, the low VCORE degrades its operating speed. To improve this problem, an overdriven <u>Sense</u> <u>Amplifier (SA) was proposed [1]</u>. However, this technique causes circuit complexity and power consumption increase. On the other hand, multi-pillar vertical MOSFET (VMOS) shown in Fig.1 was proposed [2][3]. In this paper, we propose a DRAM SA by the multi-pillar VMOS realizing 0.9V VCORE operation without overdriven technique.

2. A Sense Amplifier by Multi-pillar Vertical MOSFET

Fig.2 shows an 8F² DRAM core circuit and Fig.3 shows a SA circuit with the power supply circuit in the cross area (CA). In the conventional SA with the planar MOSFET (PLMOS), sensing speed in low VCORE is degraded drastically due to insufficient channel width, and the back bias effect owing to VPP and VBB back bias in the DRAM core circuit. The proposed SA layout with the multi-pillar VMOS relative to the SA layout with the PLMOS on the same circuit area is shown in Fig.4, and its detailed diagram is shown in Fig.5. The proposed SA realizes a 3.5 times increased channel width in the same circuit area with pitch of 8F. As shown in Fig.6 (a), drive current of SA with the multi-pillar VMOS is about 174 times larger than that with the PLMOS. Fig.6 (b) shows the normalized drive current with channel width (W_multi-pillar VMOS=W_PLMOS). From these results, the main reason of drive current improvement by the multi-pillar VMOS is its no back bias effect, even if back bias is applied as shown in Fig.6 (c).

3. Results and Discussion

The performances of the proposed SA are evaluated by HSPICE simulation. The minimum feature size is 65nm with VDD=1.2xVCORE and VPP=2.3xVDD. The BSIM4 model parameters were extracted from experimental data.

Waveforms of the conventional planar SA are shown in Fig.7. Two speed characteristics are evaluated; (1) sensing time tSA that is defined as time from VPP/2 in SAEP1 (non-overdrive) or SAEP2 (overdrive) to 0.6xVCORE of voltage difference between the two bitlines, (2) precharge time tPRE that is defined as time from 0.1xVPP in BLEQB to 0.1xVCORE of voltage difference between the two bitlines. In the planar SA, the sensing speed is degraded drastically in low VCORE, thus overdriven technique is indispensible. Waveforms of the proposed vertical SA relative to the planar SA are shown in Fig.8. The proposed

SA realizes fast sensing operation even without the overdriven technique due to the increased channel width and the back bias free characteristic of the VMOS.

The tSA vs. VCORE is shown in Fig.9. Here, Cs and Cb are cell and bitline capacitance. The dotted green line shows value of the tSA by the overdriven conventional planar SA circuit with VCORE of 1.25V. On the other hand, the proposed vertical SA improves the tSA even without the overdriven operation. The proposed SA achieves the same tSA by the VCORE of 0.75V with the overdriven operation, and VCORE of 0.9V even without the overdriven operation, relative to the conventional tSA (the dotted green line). Therefore, the VCORE is reduced from 1.25V to 0.9V, by the proposed SA without overdriven operation in the view point of the tSA. Moreover, when the VCORE is 1.25V, the overdriven proposed SA achieves 2.7ns (Cs=15fF) and 2.2ns (Cs=25fF) faster tSA than the overdriven conventional planar SA.

The tPRE vs. VCORE is shown in Fig.10. The proposed SA with the multi-pillar VMOS achieves over 0.2ns faster tPRE due to the increased channel width and the back bias free characteristic of the VMOS.

4. Conclusions

A DRAM sense amplifier (SA) circuit with the multi-pillar VMOS has been proposed. It realizes the same sensing time by VCORE of 0.9V and 0.75V without and with overdriven operation, respectively, relative to the overdriven conventional planar SA by VCORE of 1.25V. Moreover, when the VCORE is 1.25V, the overdriven proposed SA achieves 2.7ns faster sensing time than the overdriven conventional SA. Furthermore, the proposed SA achieves 0.2ns faster precharge time than the conventional planar SA. The proposed SA with the multi-pillar VMOS is suitable for sub-1V voltage and fast DRAM core operation. **Acknowledgements**

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