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A 3Gb/s Non-Contact Inter-Module Link with Duplex Transmission-Line-Couplers and Low-Frequency Compensation Equalizer

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1. Introduction

High-Speed serial inter connect transceivers have widely been used to realize reliable data transmission systems at multi-Gb/s and the beyond. For example, state-of-the-art backplane communication speed is 10.3 Gb/s at a 30-inch-long transmission line and two connectors [1]. High-speed interconnect technologies have hitherto been developed are using solid wire lines and connectors with metal contacts. In general, exposed metal terminals need strong ESD protection for devices, causing worse signal integrity and I/O power increase. On the other hand, wireless interconnect technologies are contactless but unfortunately relatively lower speed.

To solve such problems we have reported a non-contact interface scheme using transmission line couplers (TLC) [2] which could provide better signal transmitting environment, such as more accurate impedance matched conditions, to achieve 12Gb/s per a channel. However, unlike most of the previously reported structures, signals need to pass through two TLCs for backplane or system-to-system connecting applications. Therefore, signals are differentiated twice (d^2v/d^2t) and turn to double-peak pulses.

In this paper we report for the first time in the world a non-contact interconnect technique optimized to pulse-signaling associated with the 2nd order differentiation characteristics of the network. TLCs are designed to match a 50-Ohm strip-line type transmission line defined on a mother board (Fig.1).

2. TLC Inter-Module Interface

Compared with conventional wire-line connectors, TLC has following advantages; i) Built with a simple FPC or PCB pattern requiring no sophisticated mechanical structures resulting in low cost, ii) No exposition of metal terminals to lessen ESD issues. This could help to expand channel bandwidth. As reported in [2], the available frequency range is dependent on coupling length of the TLC; shorter length means higher frequency range.

Fig.2 (a) shows simulated gain-frequency characteristics for the proposed setup of non-contact inter-module link where two TLCs are located at the both ends of a 10 inch long differential FR4 transmission line. Compared with a single TLC case where signals are directly fed to the transmission line from one side, the slope is steeper. Because a TLC is constructed with the near-filed electromagnetic filed coupling between two electrodes, a 1st order differential operation is done for transmitting waves. As a result, received signals become duo-binary pulses. Therefore, in the previous report [2], a hysteresis latch was used to retrieve the data in the receiver. On the other hand, two couplers are 2nd order differential properties. Fig.2 (b) compares responses of

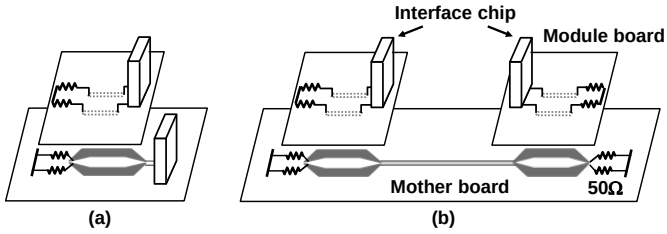


Fig.1 (a) Conventional TLC [2] and (b) Proposed duplex TLCs.

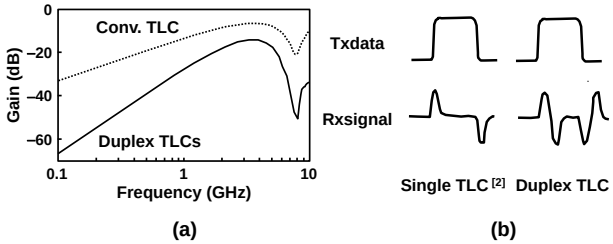


Fig.2 (a) AC response and (b) step response.

duplex TLCs and a single TLC. To retrieve the data from 2nd order differential signals by the hysteresis latch, two peaks have to be separated clearly [3]. In case the data rate is not so high, two peaks are separated clearly, but the double-peak pulse showing up in the 2nd order differentiation operation shifts the frequency spectrum higher and two peaks become indistinguishable because of the limited channel bandwidth and the hysteresis latch cannot retrieve the data.

3. Low Frequency Compensation CTLE Receiver

To receive such double-peak pulses at higher data rate we have newly developed a Low-Frequency Compensating Continuous Time Linear Equalizer (LFC-CTLE). By emphasizing the lower frequency part, signals turn to 1st order differential shapes by which hysteresis latches can operate to generate NRZ signals. The LFC-CTLE has two signal paths. One is built with linear amps plus VGAs with high-end peaking. The other is built with an LPF plus VGAs. Signals passing through those two paths are synthesized in a current summer circuit. The peaking level is adjustable in the VGA. The low-end is emphasized by an LPF and the cut-off frequency is adjustable by using varactor diode capacitors in the CR network (Fig.3 (b)). Those elements are necessary to make the receiver matched to the transmission characteristics of two-fold couplers.

Our experimental channel exhibited a 30dB/dec low-cut slope so that we have tuned the receiver to have -10dB/dec slope, resulting in a 20dB/dec slope that corresponds to the 1st order differential characteristics.

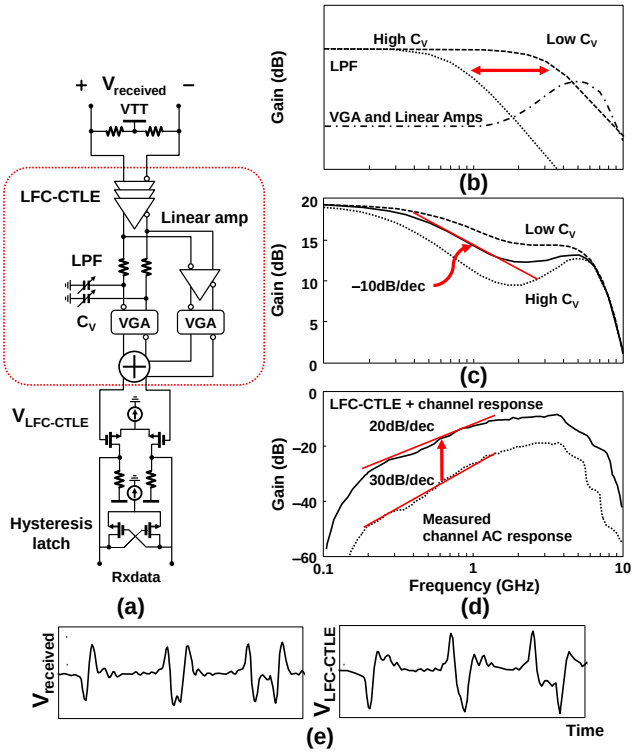


Fig.3 (a) Receiver schematic. Simulated AC response of (b) LPF and VGA, (c) LFC-CTLE AC. (d) Measured Channel AC response with and without LFC-CTLE. (e) Simulated waveforms.

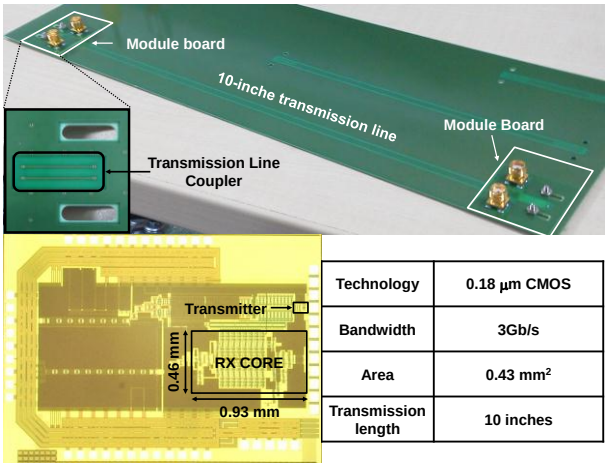
Fig.3 (e) shows simulated waveforms based on measured channel frequency-gain response. As this figure shows, the proposed equalizer turned double-peak pulses to one-peak pulses, which allows a hysteresis latch to retrieve the data at higher data rate.

4. Measurement Set Up

We have experimentally fabricated an equalizing receiver using a 0.18 μm CMOS technology where the RX core area is 0.43mm^2 (Fig.4). A 10-inch long micro strip line on a mother board is traced to bridge two transmission line couplers at both ends. The coupler is created between a module board and a mother board. The receiver is connected via SMA cables.

5. Experimental Results

An eye-diagram at the receiving point (Fig.5 (a)) shows a double-pulse shape, as we have expected, but the data could not be retrieved without or inadequate compensation of the LFC-CTLE (Fig.5 (b)). On the other hand, as shown in Fig. 5 (c), the eye clearly opens with LFC-CTLE and the bit error-rate dramatically decreases to achieve the timing margin of 0.55UI at 3Gb/s at the bit error rate of 10^{-11} (Fig. 5 (d)). However, the top-end performance was limited by the narrower first eye opening in the receiver point which was due to the loss components associated with the skin-effect and/or loss factors of the FR4 dielectric.



Technology	0.18 μm CMOS
Bandwidth	3Gb/s
Area	0.43 mm^2
Transmission length	10 inches

Fig.4 Evaluation set up and chip photo.

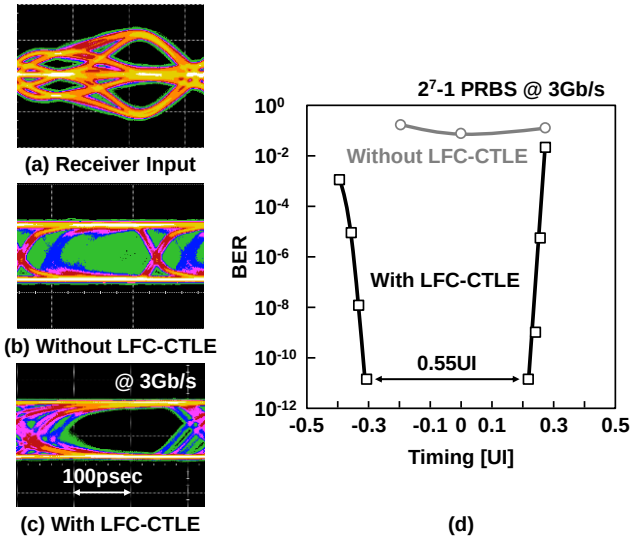


Fig.5 Measured eye diagram and bathtub curve.

6. Conclusion

Assuming flexible high-speed backplane interconnect applications, we have developed an interconnect scheme with two-fold transmission line couplers. The equalizing receiver successfully operated to detect signals of the 2nd order differentiation characteristics. The channel speed we have achieved was 3Gb/s with a 0.18 μm CMOS but this could be elevated by using advanced technologies and lower loss transmission line conditions.

Acknowledgement

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References

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[2] T. Takeya, *et. al.*, "A 12Gb/s Non-Contact Interface with Coupled Transmission Line," *IEEE ISSCC, Dig. Tech. Papers*, pp. 492-493, Feb. 2011.

[3] M. Saito, *et. al.*, "Asynchronous Pulse Transmitter for Power Reduction in ThruChip Interface," *JSAP SSDM, Extended Abstracts*, pp. 1075-1076, Sep. 2011.