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-119.1 dBc/Hz Phase Noise Ring-VCO-Based PLL CMOS Circuit Using A Tunable Narrow-Deadzone Creator in Frequency Locked Loop

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1. Introduction

Impluse-radio ultra-wideband (IR-UWB) CMOS circuits have been developed for low-power near-distance transceiver systems among silicon large-scale integrated circuits (LSI) by use of Gaussian monocycle pulse (GMP) [1, 2]. The IR-UWB signals have also been used for early-breast cancer detection systems, where short impulses are transmitted, scattered and received in the breast tissues [3, 4]. In order to calculate the impulse signal delay for confocal imaging of a cancer target, high-precision phase-locked loop (PLL) is necessary for high-speed digital sampling. Ring-voltage-controlled-oscillators (Ring-VCO) and LC-VCO have been developed [5-8]. The LC-VCO has advantages in low phase noise and low jitter but it has a disadvantage in occupied area. The ring-VCO has an advantage of small area but it has disadvantages in jitter and phase noise. Therefore, the sub-sampling PLL (SSPLL) is developed to solve the issues of the ring-VCO to suppress the jitter and the phase noise.

2. Ring-VCO-Based SSPLL

Conventional PLL

In a conventional PLL, the main loop noise sources are phase detector (PD), charge pump (CP) and divider. Due to the existence of the divide-by-N in the feedback path, the PD/CP noise is multiplied by N^2 when it is transferred to the PLL output as shown in equation (1),

$$L_{in-band,CP}(f) \approx \frac{1}{2} S_i \left| \frac{\theta_{out}(s)}{i_{cp}(s)} \right|^2 \approx \frac{1}{2} S_i \frac{N^2}{K_\varphi^2} \quad (1)$$

where Si is the power spectral density of the (thermal) noise generated by the PD/CP, $\theta_{out}(s)$ is PLL output noise transfer function, $i_{cp}(s)$ is PD/CP noise transfer function, and K_φ is the CP gain.

Sub-Sampling PLL

The sub-sampling PLL can achieve very low in-band phase noise because divider is not needed in the locked state. Fig. 1 shows a block diagram of the ring-VCO-based sub-sampling PLL. The VCO output frequency f_o is controlled by the control signal of core loop I_{cp1} and the control signal of frequency locked loop (FLL) I_{cp2}. I_{cp2} controls VCO dominantly until f_o is close to locking. When the phase error between Ref and VCO is small, it falls inside the FLL deadzone which is created by deadzone creator and FLL output becomes zero. When FLL output becomes zero, f_o is controlled by I_{cp1}. Core loop has no divider in the feedback pass so that the divider noise and its power are eliminated and the PD/CP noise is not multiplied by N^2.

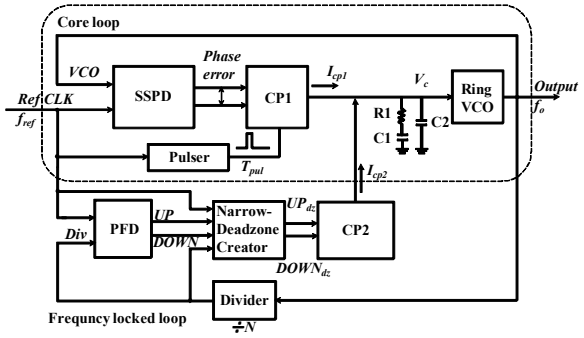
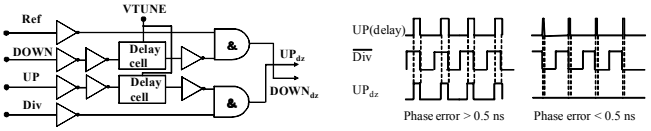


Fig. 1. Block diagram of the ring-VCO-based sub-sampling PLL.



(a) (b)

Fig. 2. Narrow-deadzone creator. (a) Schematic. (b) Timing chart.

Narrow-Deadzone Creator

The ring VCO has a large tuning gain. The small variation of VCO control voltage causes the large variation of the VCO output frequency. Therefore, the ring-VCO-based SSPLL needs a narrow-deadzone creator, and the FLL should work until f_o is further close to locking. Fig. 2 shows a schematic and timing chart of a tunable narrow-deadzone creator. It creates the timing of the deadzone +/- 0.5 ns with V_{tune} = 1.2 V. When the phase error is greater than +/- 0.5 ns, in other words, the PFD output UP/DOWN pulse widths are larger than +/- 0.5 ns, AND gates will generate the UP/DOWN pulses which are generated by PFD. When the phase error is within +/- 0.5 ns, AND gates will not geneate UP/DOWN pulse. Narrow-deadzone creator realizes ring-VCO-based SSPLL.

3. Results and Discussion

PLL Open Loop Bandwidth

The phase noise level depends on PLL open loop bandwidth f_c as shown in equation (2),

$$f_c = \frac{1}{2\pi} R1 \frac{C1}{C1+C2} K_{VCO} K_\varphi \quad (2)$$

where C1 and C2 are loop filter capacitances, K_{vco} is VCO tuning gain. Fig. 3(a) shows the dependence of measured PLL output phase noise on loop filter resistance R1. The PLL output rms jitter is translated from the phase noise *L(f)* plot as

$$\sigma_t = \frac{1}{2\pi f_o}\sqrt{2\int_{fl}^{fh} 10^{\frac{L(f)}{10}}\,df} \qquad (3)$$

where f_l - f_h is the integration region. By increasing R1 from 1 kΩ to 2.5 kΩ, the bandwidth of the loop increased and integrated rms jitter decreased from 1.48 ps to 0.925 ps (1 kHz-5 MHz).

Charge Pump Gain and Reference Frequency

The in-band Phase noise of the sub-sampling PLL circuit due to CP is shown in equation (4),

$$L_{in-band,\,CP,\,SS}(f) \approx \frac{1}{2} S_{i,\,SS} \frac{1}{K_{\varphi,\,SS}{}^2} = \frac{kT\gamma}{A_{VCO}{}^2 g_m} \frac{T_{ref}}{T_{pul}} \qquad (4)$$

where T_{ref} and T_{pul} are reference period and pulse width which is generated by the pulser respectively, γ is a noise model parameter of the MOS transistor, Avco is VCO amplitude, g_m is tranceconductance. The in-band phase noise due to SSPD is shown in equation (5),

$$L_{in-band,\,SSPD}(f) = \frac{kT}{C_{sam} A_{VCO}{}^2} T_{ref} \qquad (5)$$

where C_{sam} is sampling capacitor of SSPD. Fig. 3(b) shows the dependence of measured PLL output phase noise on K_φ. The K_φ can be controlled by T_{pul}, which determines the on-time of CP. By increasing T_{pul} from 1.3 ns to 5 ns, K_φ increased and $L_{in\text{-}band,CP,SS}(f)$ decreased. Therefore, integrated rms jitter decreased from 2.24 ps to 0.925 ps (1 kHz-5 MHz). Fig. 3(c) shows the dependence of measured PLL output phase noise on reference frequency. Measured PLL output has large phase noise from 5 MHz to 10 MHz. By increasing the reference frequency from 100 MHz to 130 MHz as T_{ref} decreased from 10 ns to 7.7 ns. The integrated rms jitter decreased from 1.84 ps to 0.725 ps (1kHz-10 MHz) because in-band phase noise is proportional to T_{ref}. The measured in-band phase noise at 1 MHz offset is –119.1dBc/Hz and integrated rms jitter is 0.725 ps.

A prototype chip was designed and fabricated in a 65 nm CMOS technology. Fig. 4 shows a chip photograph. Table I and Fig. 5 show performance comparison of ring-VCO based PLL circuits. The figure of merit (FOM) is calculated by equation (6).

$$FOM = 10\log\left[\left(\frac{\sigma_t}{1s}\right)^2 \times \left(\frac{P}{1mW}\right)\right] \qquad (6)$$

4. Conclusions

A ring-VCO-based SSPLL was fabricated in 65 nm CMOS technology. RMS output jitter which was integrated from 1 kHz to 10 MHz was 0.725 ps and in-band phase noise was -119.1 dBc/Hz at 1 MHz offset. The power consumption was 20.4 mW so that the FOM was -229.7 dB, which is the best data ever reported.

Acknowledgements

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References

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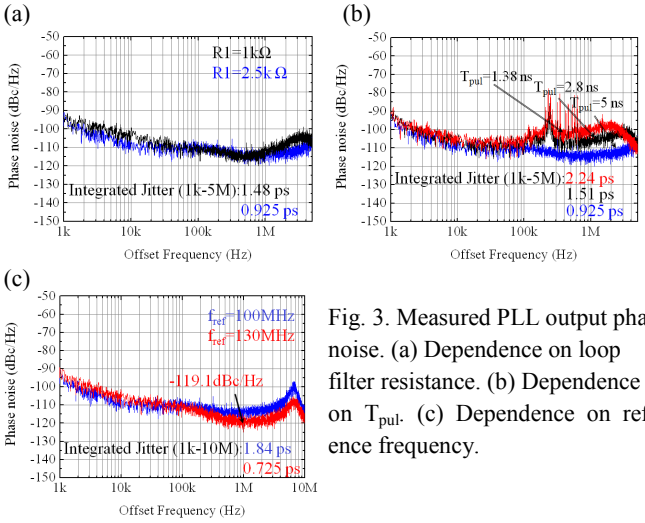

Fig. 3. Measured PLL output phase noise. (a) Dependence on loop filter resistance. (b) Dependence on T_{pul}. (c) Dependence on reference frequency.

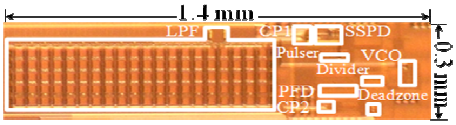

Fig. 4. Chip photograph.

TABLE I. PLL performance and comparison.

	This work	[10]	[11]	[12]
Output Frequency	2.08 GHz	1.21 GHz	2.5 GHz	3.1 GHz
Reference Frequency	130 MHz	55 MHz	100 MHz	108 MHz
(In-band) phase noise	-119.1 dBc/Hz @1MHz	-119.6 dBc/Hz @1 MHz	-106.6 dBc/Hz @1 MHz	-
Integrated jitter	0.73 ps (1k - 10M)	0.57 ps (1k - 10M)	0.99 ps (1M - 1.25G)	1.01 ps (1k-40M)
Power	20.4 mW	51.6 mW	70 mW	27.5 mW
FOM	-229.7 dB	-227.7 dB	-221.6 dB	-225.5 dB
Supply Voltage	1.2 V	1.2 V	2.5 V	1.2 V
Technology	65 nm CMOS	65 nm CMOS	45 nm SOI	65 nm CMOS

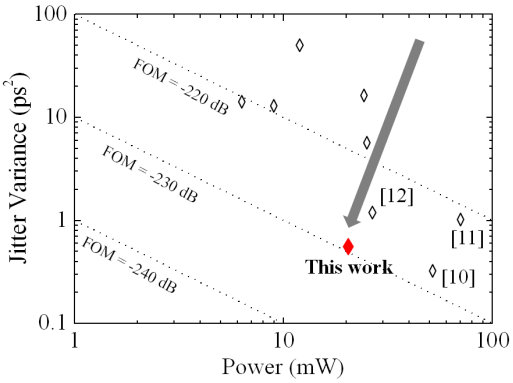

Fig. 5. Performance comparison with ring-VCO-based PLLs.

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