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150GHz Divide-by-Three CMOS Frequency Divider with Power Line Injection

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1. Introduction

Recently, reports on CMOS millimeter-wave transceivers operating above 100GHz have increased in number with the improvement of the CMOS process [1]. A frequency divider is one of the important circuits in millimeter-wave transceivers. An injection-locking technique is suitable for a frequency divider operating above 100GHz [2]. Injection-locked frequency dividers (ILFDs) are classified into two types, namely, those that use an LC oscillator (LC type) and those that use a ring oscillator (ring type). Generally, the ring type has a smaller circuit area than the LC type. However, it is difficult for the ring type to operate at high frequencies. A typical circuit diagram of a ring-type ILFD (RILFD) is shown in Fig. 1(a). MOSFETs are required to input an injection signal. However, the parasitic capacitances of the MOSFETs reduce the operating frequency of the ILFD. To solve this problem, the use of the back gate of the NMOSFET in the ring oscillator to input an injection signal was proposed [3]. The circuit diagram is shown in Fig. 1(b). A divide-by-three operation at 110GHz was realized by this method. However, it requires the use of a NMOSFET with a triple-well structure for body injection, which increases the core size. Therefore, the length of the signal line increases. It also generates large parasitic capacitances. To solve this problem, in this work, an RILFD that inputs an injection signal through power lines is proposed.

2. Proposed Frequency Divider with Power Line Injection

The circuit diagram of the proposed RILFD is shown in Fig. 2. Resistors are used as loads for NMOS inverters instead of PMOSFETs to increase the oscillation frequency and reduce the parasitic capacitances. The oscillation frequency can be adjusted using the supply voltage V_{DD}. An injection signal is input from the power lines through a bias tee. When an injection signal is input to the PILFM, NMOSFETs convert it into current. The oscillation current I_{osc} and injection current I_{inj} of each node in Fig. 2, which are in the injection-locked state, are shown in Fig. 3. The output frequency of the ring oscillator is denoted as f_0. As shown in Fig. 4, the phase of the oscillation current of each NMOSFET shifts by 120 degrees. The frequency of an injection signal that can synchronize the phase of the oscillation current of each node is three times the frequency f_0. Therefore, a divide-by-three frequency divider can be realized. The proposed RILFD does not require NMOSFETs with a triple-well structure because it uses power lines for the input. Therefore, a small circuit area can be realized. The parasitic capacitances of the signal lines decrease owing to the small circuit area. Therefore, a high operating frequency is realized. Moreover, the supply voltage of the core circuit can be set at 1.6V to further increase the operating frequency. Figure 4 shows the simulated trajectory of the drain and gate voltages of a NMOSFET in the core circuit when the supply voltage is 1.6V. As shown in Fig. 4, the maximum voltage added to the NMOSFET is approximately 1.1V, which is the process limit voltage. Therefore, the NMOSFET is not broken.

3. Measurement Results

The proposed RILFD was fabricated using the 1P8M 40nm CMOS process. The chip micrograph is shown in Fig. 5. The circuit area including the buffer was $8.8 \times 5.3\mu m^2$. The spectra of (a) free-running and (b) locked outputs are shown in Fig. 6. The supply voltages of the core circuit and buffer were 1.6V and 1.1V, respectively. As shown in Fig. 6(a), the output spectrum was broad when the RILFD oscillated at approximately 48.6GHz without an input signal. As shown in Fig. 6(b), the output spectrum became sharp when the RILFD was locked by the input signal. The input frequency was 150GHz and the input power was -3.9dBm. The output frequency was 50GHz, which is one-third of 150GHz. The locked output power was -5.6dBm, which was calibrated by the losses of a cable and a mixer. The input sensitivity as a function of operating frequency is shown in Fig. 7. The supply voltage of the core circuit was changed from 1.1V to 1.6V in steps of 0.1V. The supply voltage of the buffer was fixed at 1.1V. The input power was calibrated to the power of the probe tip. The maximum input power of -3.9dBm was limited by the maximum output power of a D-band source module. As shown in Fig. 7, the total operating frequency was 18GHz when the supply voltage of the core circuit was changed from 1.1V to 1.6V. The output waveform when the proposed RILFD was locked by the input signal is shown in Fig. 8. The phase noises of (a) free-running and (b) locked outputs are shown in Fig. 9. The phase noise of the locked output was -135.6dBc/Hz at 1MHz offset, which is an improvement of that of the free-running output. The supply voltages and input signals in Figs. 8 and 9 are the same as those in Fig. 6. When the supply voltages of the core circuit and buffer were 1.1V, the power consumption was 5.1mW, and when the supply voltages of the core circuit and buffer were 1.6V

and 1.1V, respectively, the power consumption was 12mW. Figure 10 shows a comparison of previously reported ILFDs with the proposed RILFD regarding the circuit area including the buffer as a function of the maximum operating frequency. The proposed RILFD realized the highest operating frequency among the ring-type frequency dividers and the smallest circuit area among the frequency dividers.

4. Conclusions

A divide-by-three ring-type CMOS frequency divider with power line injection operating above 150GHz was proposed. The circuit area of the proposed RILFD was the smallest among all the frequency dividers considered in this study, and the operating frequency of the proposed RILFD was 151.3GHz, which is the highest value obtained among the ring-type frequency dividers.

Acknowledgements

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References

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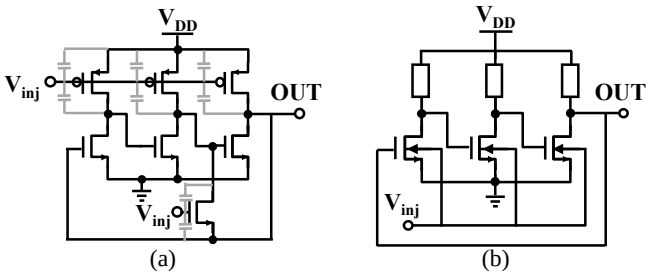

Fig. 1 Circuit diagrams of (a) RILFD with input MOSFET and (b) RILFD with body injection.

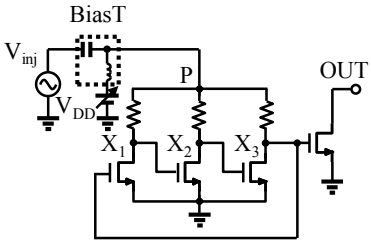

Fig. 2 Circuit diagram of proposed RILFD.

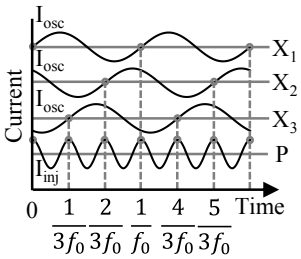

Fig. 3 Current waveforms of nodes in Fig. 2.

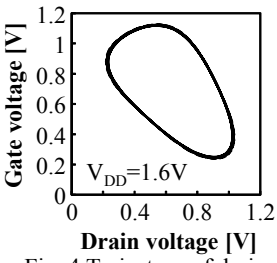

Fig. 4 Trajectory of drain and gate voltages of NMOSFET.

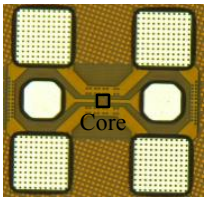

Fig. 5 Chip micrograph.

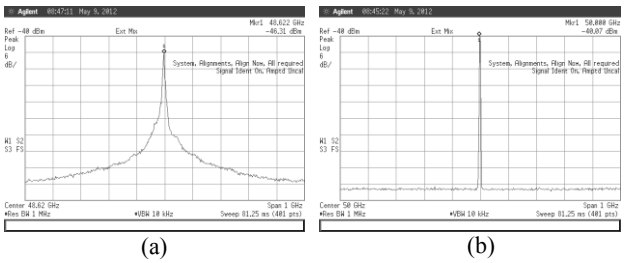

Fig. 6 Spectra of (a) free-running and (b) locked outputs.

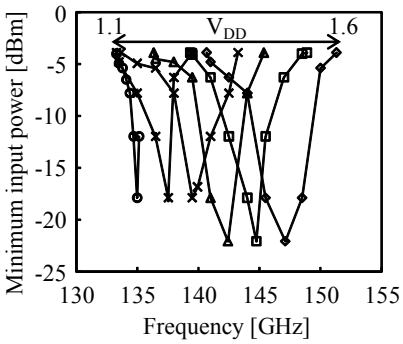

Fig. 7 Input sensitivity of proposed RILFD.

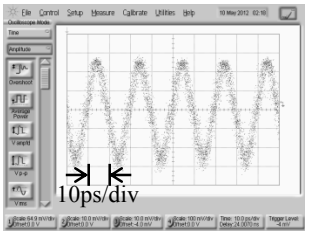

Fig. 8 Locked output waveform when input signal of 150GHz was injected.

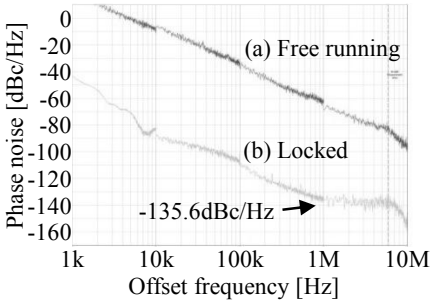

Fig. 9 Phase noises of (a) free-running and (b) locked outputs.

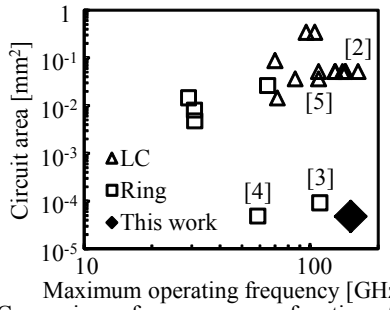

Fig. 10 Comparison of core areas as a function of frequency.