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Fractionally Injection-Locked Frequency Multiplication Technique with Multi-Phase Ring VCO

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1. Introduction

Injection-locked frequency multipliers (ILFMs) are attractive since they can easily obtain low-phase-noise frequency-multiplied outputs only with an additional simple circuit. In conventional ILFMs, however, there is an disadvantage that output frequencies (f_{out}) are limited by integral multiple of the injection frequency (f_{inj}), i.e. $f_{out} = f_{inj}$, $2 \times f_{inj}$, $3 \times f_{inj}$,… In those cases, the frequency resolution step is f_{inj}. Generally, low-frequency references are required to improve the frequency resolution, although it has poor phase noise. This is because superharmonics of the references do not have large enough power to widen the lock range [1].

This paper proposes a novel fractionally injection locked frequency multiplication technique, which can achieve not only fine output frequency resolution but also good phase noise. The proposed ILFM applies multiple injections into a multi-phase VCO to realize the technique.

2. Fractionally Injection-Locking Technique

Fig. 1 shows the proposed ILFM that is based on a 6-stage differential ring VCO. Delay cell proposed in our previous work are applied [2]. This circuit employs a direct injection technique to inject the cyclic external force since the technique is preferable for its simple topology and wide lock ranges [3]. Rail-to-rail reference pulses are injected into nMOS switches to short ILFM differential outputs.

Fig. 2 (a) shows time-domain waveforms of 1/2-integral frequency multiplication ($T_{inj} = 5/2 \times T_{out}$) [4]. Two differential output nodes (V_{out}, V_{outb}) are shorted when the injection signal V_{inj} is input into an nMOS switch. In Fig. 2 (a), there are two zero-crossing points of VCO outputs which can be shorted over the VCO period (T_{out}). As a result, rising and falling edges of VCO outputs can lock to the pulses in turn, and accumulated phase error can be reset. In this case, 1/2-integral and integral frequency multiplication can be achieved by adjusting VCO output frequencies to follow the equation of $f_{out} = (N+1) / 2 \times f_{inj}$ (N=1, 2, 3, …).

Fig. 2 (b) shows time-domain waveforms of the proposed ILFM with injecting V_{inj1}, when 1/4-integral frequency multiplication would be achieved. In this case, injection pulses into two switches (V_{out1}-V_{out1b}, V_{out4}-V_{out4b}) short two pairs of differential output nodes. However, lock condition cannot be achieved when the pulse width is wide. This is because injections input into peak-to-peak ILFM outputs cause phase rotation of the nodes and phase unbalance between the differential-output pairs. On the other hand, when the pulse width is narrow enough, lock condition can be achieved since the force causing phase error by injection can be neglected, compared with the force maintaining phase balance by oscillation among all ILFM outputs [5]. Therefore, 1/2-integral subharmonic locking phenomena as shown in Fig. 2 (a) are observed in each ILFM output pair (V_{out1}-V_{out1b}, V_{out4}-V_{out4b}) neglecting the injections into peak-to-peak ILFM outputs ($2 \times T_{inj1} = 5/2 \times T_{out1}$). As a result, 1/4-integral frequency multiplication can be achieved by combining the effective injections of two pair of differential outputs ($T_{inj1} = 5/4 \times T_{out1}$). In this case, accumulated phase error would be reset twice as much as the case of the single injection [5].

Fig. 2 (c) shows the case of 1/3-integral frequency multiplication ($T_{inj2} = 4/3 \times T_{out2}$). As the case of 1/4-integral frequency multiplication, 1/3-integral frequency multiplication is obtained when the outputs (V_{out1}, V_{out3b}, V_{out5}) are simultaneously shorted by injected pulses (V_{inj2}).

The proposed ILFM has capability to lock 1/6-integral subharmonics of the references because there are differential coupling via latches. The effective injections input into each switch can lock to rising and falling edges of an ILFM output pair in turn as the case in Fig. 2 (a).

3. Measurement Results

To confirm the proposed technique, the ILFM shown in Fig. 1 was fabricated in 180 nm CMOS process, and measured with 1.4-V power supply voltage. Fig. 3 shows a chip micrograph of the ILFM, whose core area is 150 × 260 μm^2. As reference signals, external 100-MHz pulses with 83.3-ps width were input. When the frequency tuning voltage was swept, 1/2- and 1/4-integral frequency multiplications were observed by injecting V_{inj1} as shown in Fig. 4 (a). 1/3- and 1/6- integral frequency multiplications were observed by injecting V_{inj2} as shown in Fig. 4 (b).

Fig. 5 (a) shows phase noise at f_{out} = 725 MHz (=100×29/4) without and with injection (V_{inj1}) when f_{inj} = 100 MHz. The phase noise at 1-MHz offset was -120 dBc/Hz. Fig. 5 (b) shows phase noise at f_{out} = 767 MHz (100×23/3) without and with injection when f_{inj} = 100 MHz (V_{inj2}). Measured phase noise at 1-MHz offset was -119 dBc/Hz.

4. Conclusions

A fractionally frequency multiplication technique with injection locking was proposed. The technique was experimentally verified by using a 6-stage differential ILFM and multiple injections. 1/2-, 1/3-, 1/4-, and 1/6-integral and integral frequency multiplication accompanying phase noise reduction could be realized with the proposed ILFM.

Acknowledgements

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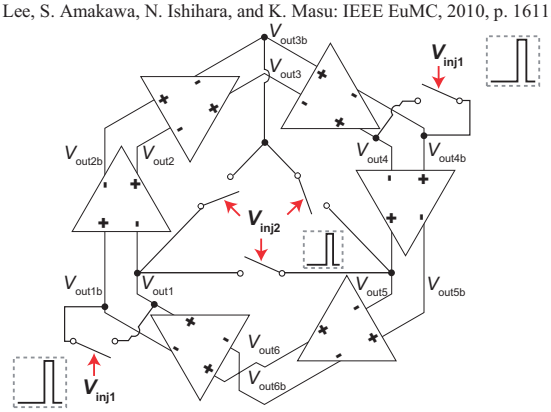

Fig. 1 Proposed ILFM.

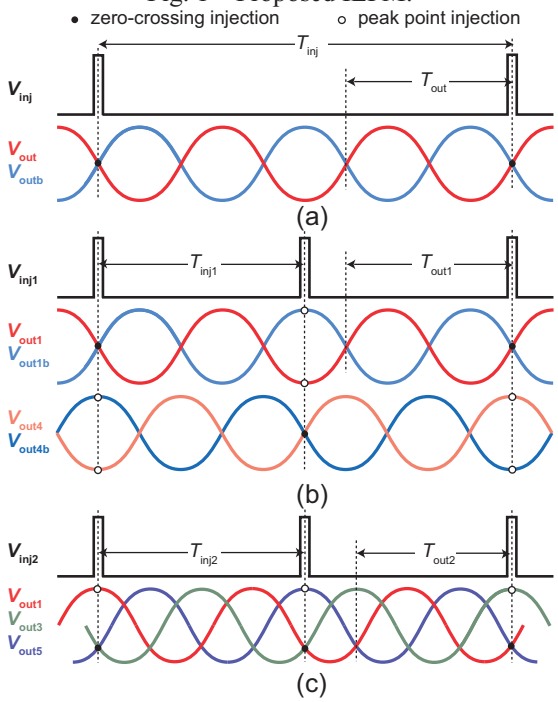

Fig. 2 Voltage waveforms of ILFM outputs and injection signals versus time; (a) 1/2-, (b) 1/4-, and (c) 1/3- integral frequency multiplication.

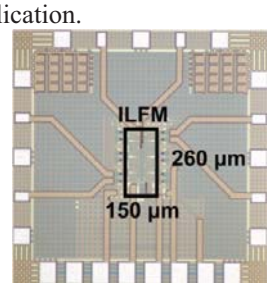

Fig. 3 Chip micrograph.

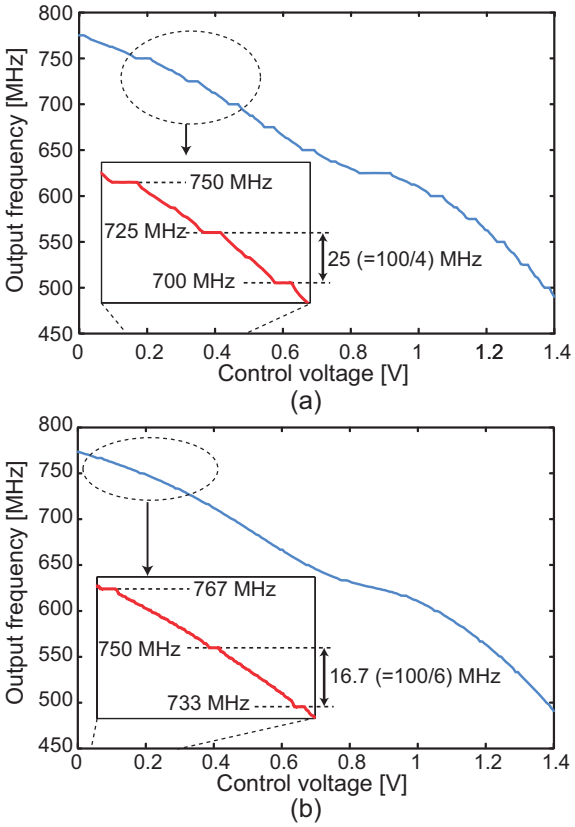

Fig. 4. Tuning range with the 100-MHz-reference signal; (a) 1/2-, 1/4-integral, and (b) 1/3-, 1/6-integral frequency multiplication.

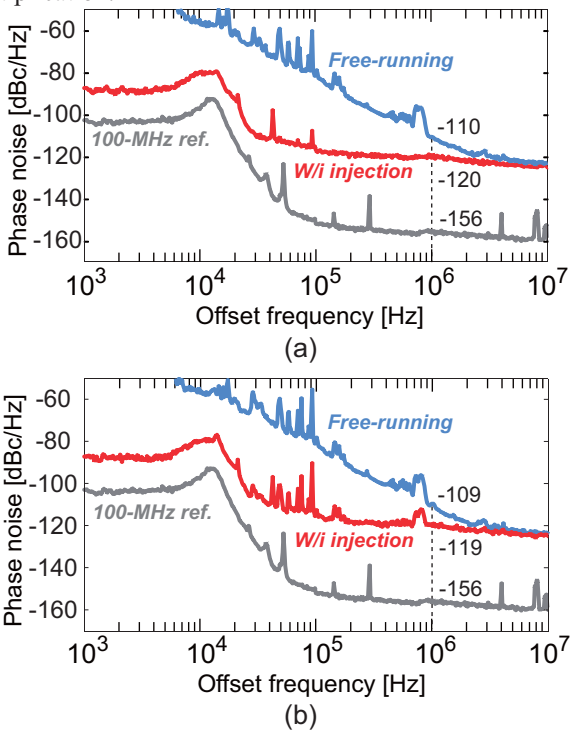

Fig. 5 Measured phase noise characteristics (a) at f_{out} = 725 MHz without and with injection locking (f_{inj} =100 MHz), (b) at f_{out} = 767 MHz without and with injection locking (f_{inj} = 100 MHz).