Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp1160-1161

Analysis and Design of Coil with Feed Line for ThruChip Interface

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1. Introduction

ThruChip Interface (TCI) is a low-cost and high-performance wireless interface between three-dimensionally (3D) stacked chips in a package. TCI communicates through inductive coupling between on-chip metal coils made by IC interconnections. The TCI coils can be placed almost anywhere even over a memory core [1], yielding following three benefits. 1) The number of channels can be increased for high bandwidth, 2) larger coils can be placed for power reduction or range extension, or 3) the coil position can be directly aligned without an interposer [2] for low cost. However, the transceiver circuit position is sometimes limited especially in a memory chip. In this case, the transceiver and the coil are connected through long feed lines as shown in Fig.1. This long feed line would cause additional parasitics to the coil and may degrade the performance. In this paper, an equivalent circuit model for analysis and a simple design guideline for the coil with long feed line are proposed. Modeling accuracy and design validity are evaluated by test-chip measurement in 0.18μm CMOS.

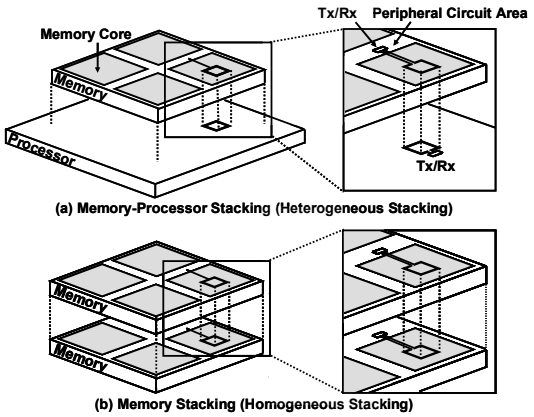

Fig.1 Coils with long feed lines in ThruChip Interface for (a) memory-processor stacking and (b) memory stacking.

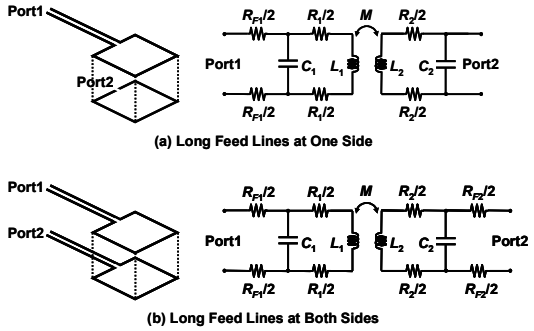

Fig.2 Equivalent inductive-coupling channel model with long feed lines at (a) one side and (b) both sides.

2. Analysis and Design Guideline

Fig.2 depicts the equivalent circuit models of the coil with long feed lines. One (Fig.2(a)) is for long feed lines at one side of the coil (Case.A) and the other (Fig.2(b)) for both sides (Case.B). The long feed lines can be modeled as additional parasitic resistance (R_F) and capacitance (included in parasitic capacitance of the coil C_1 or C_2). Increase in the parasitic capacitance will decrease the resonant frequency of the coil f_{SR} and hence channel bandwidth [3]. In order to keep constant bandwidth, the coil inductance L is reduced by reducing the number of coil turns n. For the 400μm-diameter coil in 0.18μm CMOS, the optimal n is designed to be 4 based on the design guideline [3]. n is reduced to 3 and 2 for 250μm and 700μm feed line length so that the f_{SR} and the channel bandwidth can be kept constant as shown in the simulated result in Fig.3. However, due to the reduction in L, trans impedance (coupling strength) of the channel is reduced as mutual inductance M is given by $k(L_1L_2)^{0.5}$ where k is coupling coefficient. This reduction in the trans impedance can be compensated by additional transmit current I_T since V_R is proportional to MI_T. Since L is proportional to n^2, I_T is increased by the turn ratio. In case of 250μm feed line length, I_T is increased to 4/3 (=1.33) in Case.A and 16/9 (=1.78) in Case.B. In case 700μm, 4/2 (=2) and 16/4 (=4) respectively. This is the worst-case scenario. In reality, L is proportional to n^{α} ($1<\alpha<2$). In addition, the coil line width can be widened for a constant quality factor of the coil Q (Q determines ringing in V_R pulse and Inter-Symbol Interference (ISI) [3]). The wider line width improves the coupling coefficient k. By reducing n to one, the feed line can be extended to 2,400μm. Based on the worst-case scenario, I_T should be increased to 16/1 however practically 10x increase in I_T is sufficient enough due to this line width optimization.

3. Test-Chip Measurement

Test chips are designed and fabricated in 0.18μm CMOS. Fig.4 shows the stacked test chips. One (Fig.4(a)) is for evaluating long feed lines at one side. The other (Fig.4(b)) for both sides. The upper chips are thinned down to 100μm and stacked with 10μm glue. The communication distance is therefore 110μm. Four kinds of coils are integrated whose coil turns n=4 without feed lines, n=3 for 250μm feed lines, n=2 for 700μm feed lines, and n=1 for

1,350μm feed lines. Due to chip area limitation, feed line length of the single-turn coil is shortened.

Fig.5 presents measured BER dependence on transmit power. 2^7-1 Pseudo-Random Binary Sequence (PRBS) is used as a test pattern. All the coils including the single-turn coil with 1,350μm are successfully operate with BER<10^{-12} at 2Gb/s. Additional transmit power required for BER<10^{-12} is measured in 6 samples and averaged. Fig.6 summarizes the measured additional transmit power dependence on feed line length. Good agreement between measurement and calculation is obtained.

4. Conclusion

Equivalent circuit models for the coil with the long feed line are proposed. The effect of the feed line is analyzed and the design guideline for the coil with the feed line is explained. The accuracy and validity of the analysis and design guideline are verified by test-chip measurement.

Acknowledgements

This work is supported by CREST/JST.

References

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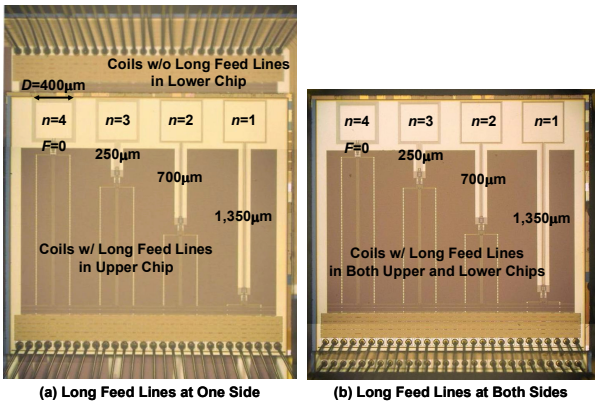

Fig.4 Stacked test-chips in 0.18μm CMOS for (a) long feed line coil at one side and (b) both sides.

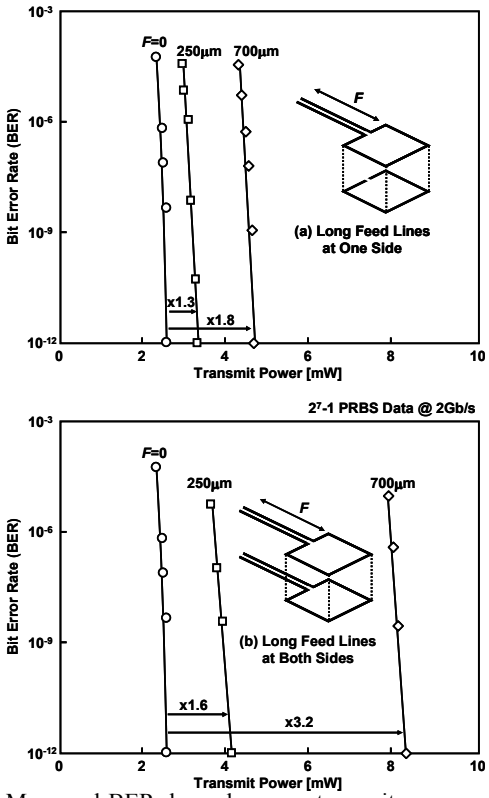

Fig.5 Measured BER dependence on transmit power with long feed lines coil at (a) one side and (b) both sides.

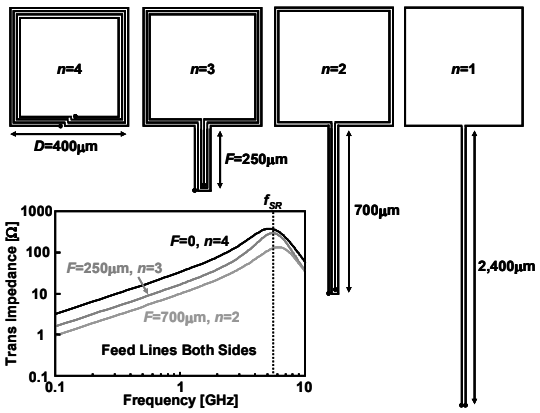

Fig.3 Coil layout and simulated trans impedance for different feed line length.

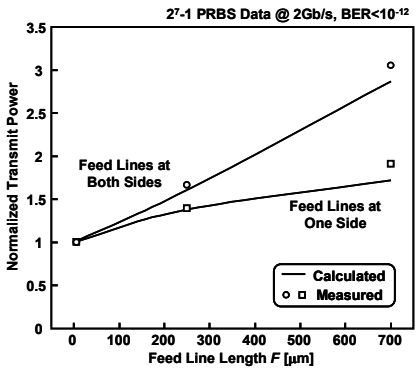

Fig.6 Measured and calculated additional transmit power dependence on feed line length.