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THz Matrix-Based Layered Wrapper Model of Common-Source MOSFET

Kosuke Katayama[1], Mizuki Motoyoshi[1], Kyoya Takano[1], Suguru Fujita[2] and Minoru Fujishima[1]

[1]Graduate School of Advanced Sciences of Matter, Hiroshima University
1-3-1 Kagamiyama, Higashi-Hiroshima, Hiroshima 739-8530, Japan
Phone: +81-82-424-7641, Fax: +81-82-424-4508, E-mail: katayama@dsl.hiroshima-u.ac.jp
[2]Tokyo R&D Center, Panasonic Corporation
600 Saedo-cho, Tsuzuki-ku, Yokohama City, 224-8539, Japan

1. Introduction

Terahertz (0.3-3THz) CMOS circuits and applications are have been developed [1, 2]. In other frequency bands, providing an accurate MOSFET model is important for designing circuits. We have proposed a matrix-based wrapper model [3, 4], which covers up to the D-band (170GHz) by directly distinguishing the measured and PDK model (M_{LOGIC}) as a matrix by taking into account non reciprocal propagation (Fig. 1). However, this model is not applicable for a THz circuit design because its frequency response has resonances (Fig. 2). These resonances are caused by the high-order s-domain polynomials of admittances (y_{in}, y_r, y_f and y_{out} in Fig. 1). In this paper, we propose a method of reducing the order of polynomials and introduce a model with a smooth frequency response up to 300GHz. The high complexity of the model originates from the fact that admittances are forced to account for all elements not associated with MOSFETs, such as lead lines made of coplanar waveguides. Thus, we applied the two-step open-short de-embedding method [5] to extract the core MOSFET from the measured device. In section 2, a matrix-based layered common-source MOSFET model using the open-short de-embedding method is introduced. In section 3, the frequency responses of this model are shown and compared with the measured results.

2. Matrix-Based Layered Common-Source MOSFET Model Using Open-Short De-Embedding Method

Figure 3 (a) shows a matrix-based layered common-source MOSFET model. To extract the core of the MOSFET model (Fig. 3 (b)), open (Fig. 3 (c)) and short (Fig. 3(d)) models are defined [5]. In Fig. 3, the wrapper (Y_{wrap}), which is composed of y'_{in}, y'_m, g_m and y'_{out}, compensates the difference between the PDK model (Y_{LOGIC}) and measured core value (Y_{core}). The elements are derived as

$$\begin{cases} y'_{in} = y_{11} + y_{12} \\ y'_m = -y_{12} \\ g_m = y_{21} - y_{12} \\ y'_{out} = y_{12} + y_{22} \end{cases} . \tag{1}$$

The measured value is reduced by open (Z_{open}) and short (Z_{short}) values. Each branch of these models is also calculated as a matrix coordinated to the measured frequencies. Finally, the matrices are fitted to the s-domain rational polynomial functions by the least-squares method [4].

3. Comparison with Measured Results

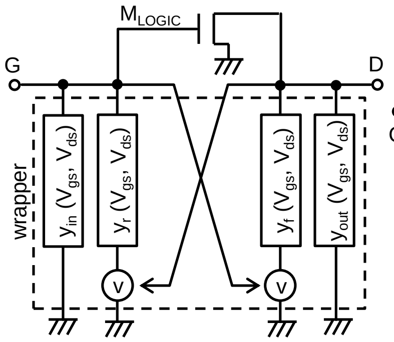
A MOSFET device was fabricated using 40nm CMOS technology (Fig. 4(a)). Its W/L is 120μm/40nm. Its gate, drain and source are connected to the left, right and ground pads, respectively. Its gate and drain biases are supplied via bias tees. Open (Fig. 4(b)) and short (Fig. 4(c)) devices were also fabricated. The open device layout is realized by simply removing the gates of the MOSFET device. The short device layout is realized by connecting all the internal nodes of the open device. After measuring the devices using VNA, the pads of the devices are de-embedded by the TRL method [6]. By applying the procedure described in the preceding section, the s-domain rational polynomials of the branches are obtained. The orders of the rational polynomial functions are suppressed in comparison with those of a single-layered matrix-based common-source MOSFET device model (Fig. 1). Figure 5 shows the scattering parameters of the measured (symbols) and modeled (lines) MOSFET results. The model, which is a core model embedded by open and short models, is calculated using a circuit simulator. The obtained result confirms that this model matches the measured results well. Moreover, unexpected resonances do not exist up to 300GHz.

4. Conclusions

In this paper, we introduce a novel model of a matrix-based layered common-source MOSFET, whose layers contribute to the reduction in the s-domain complexity of branches and unexpected resonances. The reliability of this model was confirmed by the comparison of measured and simulated results.

References

[1] K. Sengupta, et al., ISSCC, pp. 256-258, Feb. 2012.
[2] Y. M. Tousi, et al., ISSCC, pp. 258-260, Feb. 2012.
[3] K. Katayama, et al., TJMW 2011, pp. 4-7, 2011.
[4] K. Katayama, et al., IEICE TRANS. ELECTRON, Vol. E95-C, No. 6, Jun. 2012.
[5] ZM. Koolen, et al., Bipolar Circuits and Technology Meeting, pp. 188-191, Sept. 1991.
[6] G. F. Engen, et al, IEEE Trans. on Microwave Theory and Techniques, Vol. 27, No. 12, Dec. 1979.



$$Y_{wrap} = Y_{meas} - Y_{LOGIC}$$

Fig. 1. Single-layered matrix-based common-source MOSFET device model.

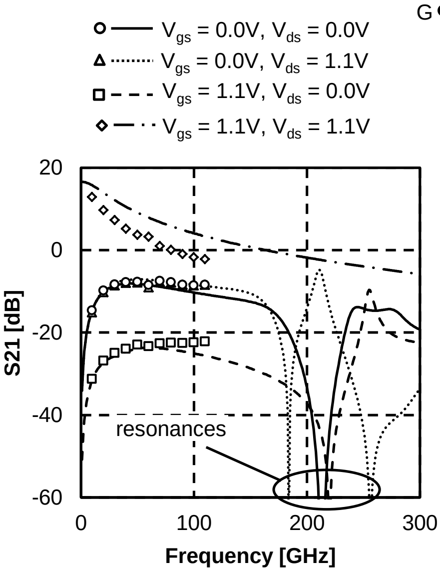
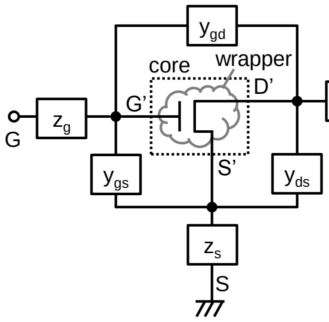
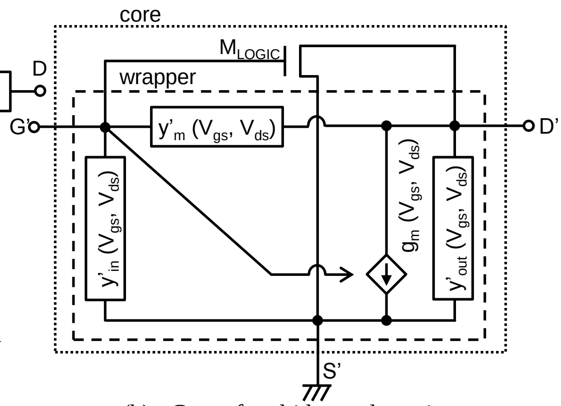


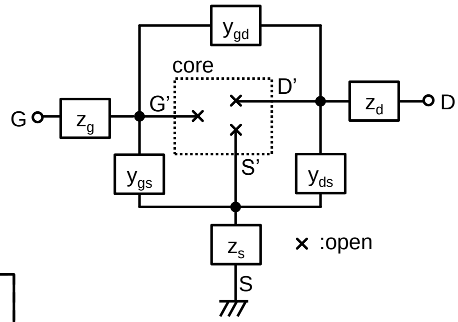
Fig. 2. S21 values of the measured (symbols) and matrix-based wrapper (lines) model at various bias voltages and frequencies. Some resonances can be observed in the model.



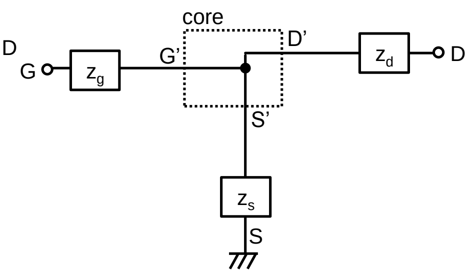
(a) Multi layered matrix-based MOSFET device model.



(b) Core of multi layered matrix-based MOSFET device model.



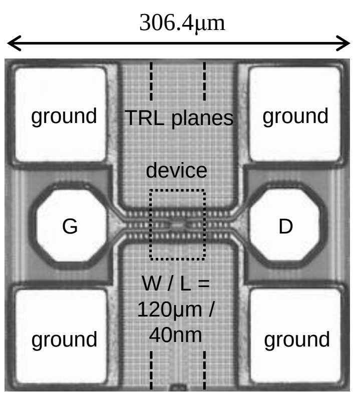
(c) Open device model.



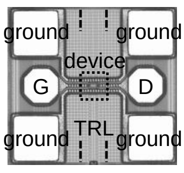
(d) Short device model.

$$Y_{core} = \left(Z_{meas} - Z_{short}\right)^{-1} - \left(Z_{open} - Z_{short}\right)^{-1}, Y_{wrap} = Y_{core} - Y_{LOGIC} = \begin{pmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{pmatrix}$$

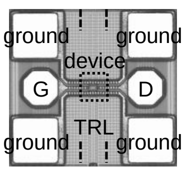
Fig. 3. Multi layered matrix-based common-source MOSFET device model and open-short device models used for core de-embedding.



(a) MOSFET device.



(b) Open device.



(c) Short device.

Fig. 4. Chip micrographs of devices. These devices use same pads and have same TRL planes.

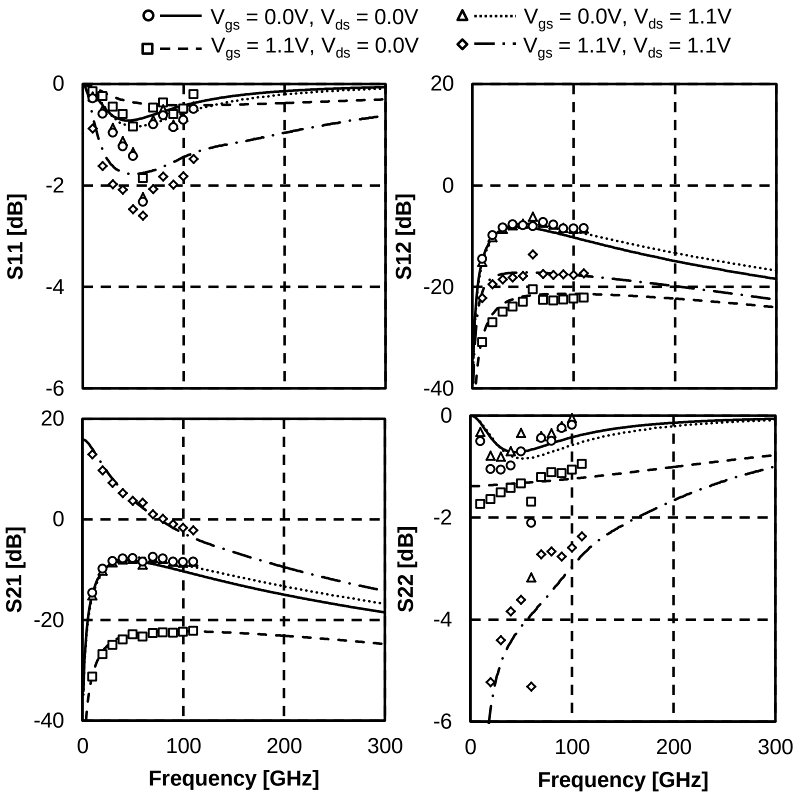


Fig. 5. Measured (symbols) and modeled (lines) scattering parameters at various biases as a function of frequency.