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Integrating carbon nanotubes as vias in a monolithic 3DIC process

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1. Introduction

Monolithic 3D integration offers device level 3D integration for integrated circuits with dense vertical interconnects (vias) [1]. For the vias in monolithic integrated ICs Cu is a less attractive material, due to reliability issues for high aspect ratio Cu vias and potential contamination of the device layers.

Carbon nanotubes (CNT) can be an attractive candidate as via material in 3D IC. They offer good electrical reliability [2] and high aspect ratios, combined with a superior thermal conductivity as high as 3500 W/mK [3]. Much interest has already been shown in using CNT as via material in future 2D IC [4-7].

Recently we proposed the use of a bottom-up approach to integrate CNT into a monolithic 3D IC process [8]. The biggest advantage of this approach is that no metal deposition into high-aspect ratio (HAR) holes is required, and it allows the use of bundle densification techniques. Beside the bottom-up method we also investigated the traditional top-down approach, which we found to be also suitable for high-density (10^{11} tubes/cm^2) low temperature (500°C) multi-walled CNT growth [9].

In this paper we report on the electrical properties of CNT vias measured using 4-point probe measurements structures for both the top-down and bottom-up process. After that we display successful CNT growth on transistor layers suitable for a monolithic 3D IC process.

2. Experimental

CNT are grown using a commercial AIXTRON BlackMagic* low-pressure chemical vapour deposition (LPCVD) reactor at 80 mbar on 4" wafers using 5 nm Fe as catalyst. As support later underneath the catalyst TiN is used, which is a standard barrier material in semiconductor processing. First the catalyst is annealed for 3 min. in 700 sccm H_2 at 500°C, followed by the addition of 50 sccm C_2H_2 for a specific time to achieve the desired CNT length.

The exact process for measurements structure fabrication can be found elsewhere [8, 9]. In order to achieve good contact to the CNT Ti and TiN is used as contact material. It is important to note that we found that TiN as support material for the catalyst is sensitive to plasma damage during for instance oxide etching. To prevent damage to this layer we employ a sacrificial Ti layer which is removed using short wet etching in 0.55% HF.

The details of our thin-film transistor (TFT) 3D IC process can be found elsewhere [1, 10]. In short: using an excimer laser an a-Si film deposited using (LPCVD) at 545 °C is crystallized in order to form 6-8 µm Si grains in which TFT are fabricated. The implanted dopants are activated using excimer laser annealing Using SiO_2 as dielectric multiple layers of TFT can be fabricated in order to form circuits.

3. Results and discussion

In fig. 1 a cross-section of a 2.5 µm long CNT via fabricated using a top-down process can be found prepared using a dual-beam SEM/FIB system. As can be seen the CNT are well-aligned. The diameter of the multi-walled CNT is estimated to be 10-15 nm, with a density of 10^{11} tubes/cm^2. The top contacts are embedded in the Ti contact layer, which we found to allow the formation of a good metal-CNT contact [11].

Using a 4-point probe structure the CNT vias were electrically characterized for both the top-down as bottom-up process. For both the top-down as bottom-up process the IV-curves are displayed in fig. 2. While the top-down process shows a linear response, indicating good Ohmic contact, the bottom-up process displays a small Schottky contact. We suspect this is caused by the top-contact, which is different between both processes. For the top-down process contact area is large, while it is small for the bottom-up process.

From the measured via resistance and geometry we calculated the CNT bundle resistivity and compared them with values found in literature, as shown in fig. 3. As can be seen our values are among the best values in literature, while our deposition temperature of 500°C is lower than that of Kreupl et al., Dijon et al. and Choi et al.

Our next step is to integrate the layers and steps required to fabricate CNT vias into our monolithic 3DIC TFT process. Normally, Al or poly-silicon is used for metallization. However, Al cannot survive the growth temperature used for the CNT, while we cannot grow CNT directly on poly-silicon due to catalyst diffusion. We decided to change to a process using Ti and TiN for all metal layers (i.e. gate and metal contacts to the source and drain of the TFT). This offers several advantages: first of all Ti/TiN easily survives the CNT growth temperature (and also LPCVD a-Si deposition). Furthermore, the sheet resistance of Ti, albeit higher than that of Al, is lower than that of poly-silicon. Most importantly, we can directly grow CNT on these metal layers, which also function as diffusion barrier for the Fe into the active transistor region.

Using this process we successfully grew CNT on top of both the gate Ti/TiN stack (with TiN on top) as the source/drain Ti/TiN contact pads. Both layers were protected using Ti during processing, which were removed just before Fe catalyst deposition. The resulting CNT are displayed in fig. 4.

The process can be applied to fabrication of a 3DIC device using two layers of TFT which will use CNT as vias between both transistor layers.

4. Conclusions

We are able to grow CNT using both a top-down and bottom-up process, both showing a relative low resistivity around 10 mΩ-cm. The bottom-up process has non-ideal top contacts, while the top-down process displays excellent Ohmic contact. We successfully were able to grow CNT directly on Ti/TiN gate and source/drain metal of the tin-film transistor layer.

Acknowledgements

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*The identification of commercial products is to specify the experimental conditions and does not imply any NIST endorsement or recommendation of that they are necessarily the best for the purpose.

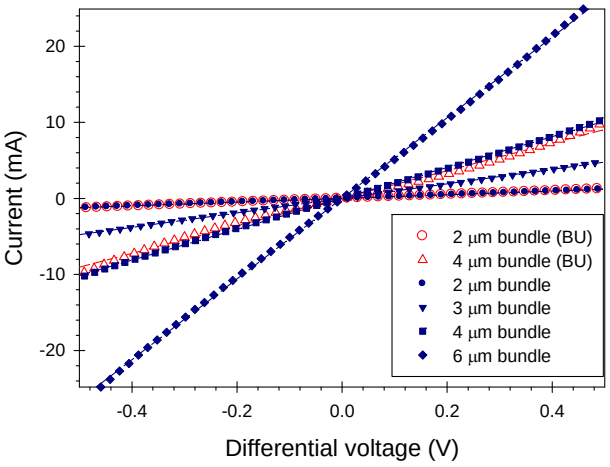

Fig. 2: Measured I-V characteristics of CNT vias fabricated using a top-down (blue, closed symbols) and bottom-up (BU, red, open symbols) process.

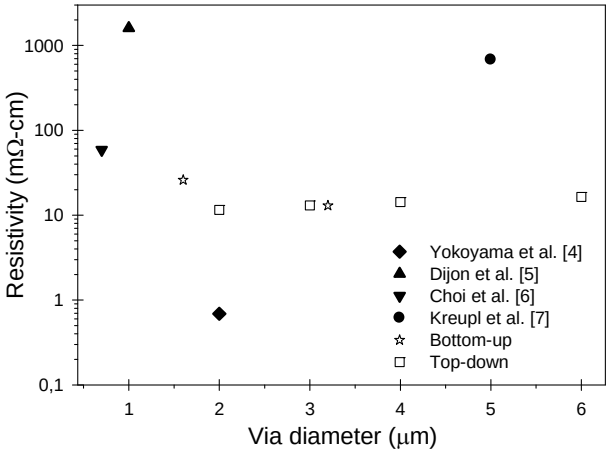

Fig. 3: Calculated resistivity's for the top-down and bottom-up process compared to values from literature.

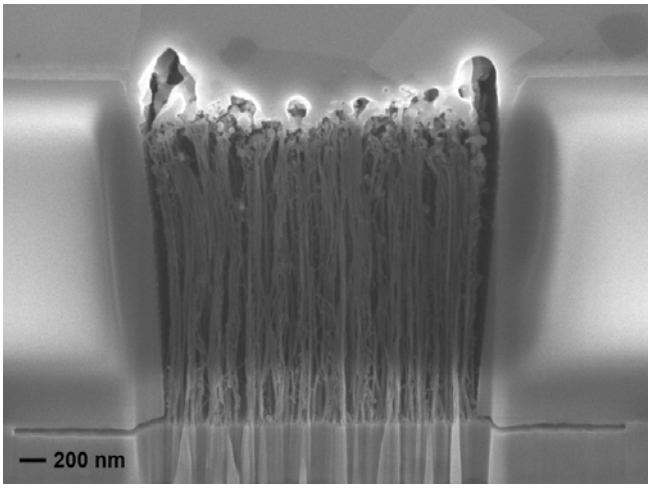

Fig. 1: FIB SEM cross-section of 2 μm wide and 2.5 μm long CNT via.

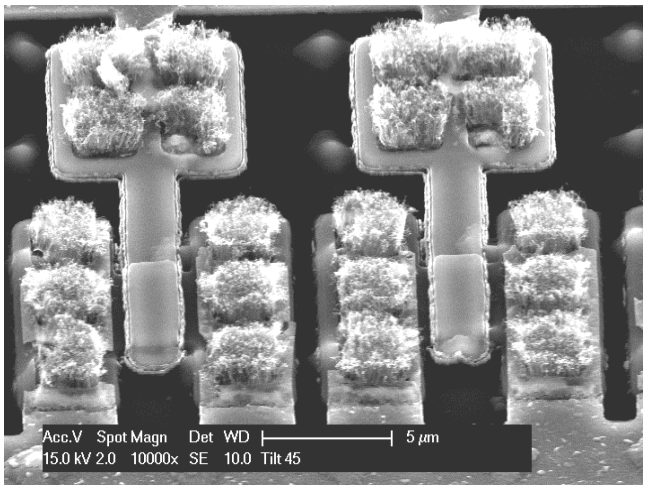

Fig. 4: SEM of CNT directly grown on gate metal and source/drain contact area.