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Sub-micron-accuracy Gold to Gold Interconnection Flip-Chip Bonding Approach for Electronics-Optics Heterogeneous Integration

T. T. Bui, L. Ma, M. Suzuki, F. Kato, S. Nemoto, N. Watanabe and M. Aoyagi

National Institute of Advanced Industrial Science and Technology
1-1-1 Umezono, Tsukuba, Ibaraki 305-8568 Japan
Phone: +81-2-9862-6510 E-mail: m-aoyagi@aist.go.jp

1. Introduction

The major progress in electronics-optics heterogeneous integration which has been achieved in the last few years has highlighted the challenge represented by the interfacing and packaging of these new systems [1]. In electronics-optics heterogeneous integration applications, optical performance of a system is mainly dependent on the waveguide-to-device coupling technique (Fig.1). Matching the light field of the component to the mode field of the other component (e.g. from an exciter to a waveguide) is needed for efficient transferring of optical energy. The coupling efficiency is mainly affected by the numerical aperture of waveguides, refractive index changes, and offsets (Δx, Δy, Δz) [2]. Therefore, coupling losses caused by the offsets are critical. The optical connections should confirm mechanical tolerances of 1 μm or less in order to achieve acceptable coupling loss.

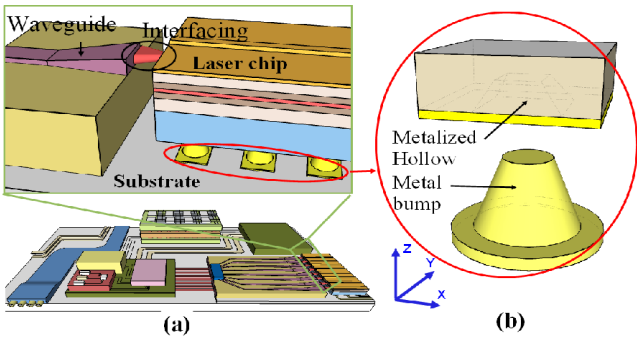

Fig. 1 Electronics-optics heterogeneously integrated module (a) and proposed gold to gold interconnection (b).

One of candidate techniques for electronic and optical heterogeneous integrated system is flip chip bonding technique with fine bumps, which enable multiple stacking of many advanced semiconductor devices such as three-dimensional integrated circuit (3D IC). However, the bonding accuracy of presently commercialized flip chip bonding machines has been limited to the range of 2–5 μm. It is clear that new integration techniques are required to bring advanced electronics-optics integration system into actual applications. Up to now, many techniques have been studied to improve the accuracy of bonding. Bonding accuracy up to 100 nm has been obtained [3]. However, due to the fact that the technique requires a realignment process after each down-force step, it is likely very time consuming for an alignment and bonding processes.

In this paper, an advanced flip chip bonding technique using gold truncated cone bump and gold-deposited hollow pyramid structures pair is developed for aiming at sub-micron range precision alignment based on the self-alignment effect.

2. Bonding approach and test sample design

The technique using in this work is based on using bump (convex) and hollow (concave) elements pair (Fig.1(b)), to align a chip to a substrate during stacking. First, by a commercialized bonding machine, a chip is picked-up and aligned with a substrate. After that, bonding treatments (i.e. heating, compressing) are applied to create strong bump joints. Bump and hollow structures in this case will provide mechanical guides, i.e the sloped sidewalls of the dielectric pyramids help guide the top die cone bumps to substrate bonding target, for maintaining high precision alignment between the interconnect pads during the bonding process (Fig.2). Transverse offsets Δx, Δy, and angular offset Δθ are guaranteed by the bump and hollow pair structure while longitudinal offset Δz is decided by controlling the height of a stopping structure.

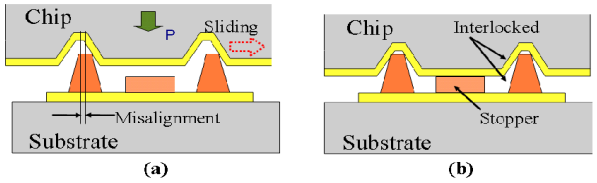

Fig. 2 Drawings show the working principle of proposed misalignment self-correction pair structure. Bump and hollow structures provide mechanical guides for maintaining high precision alignment between the interconnect pads during the bonding process.

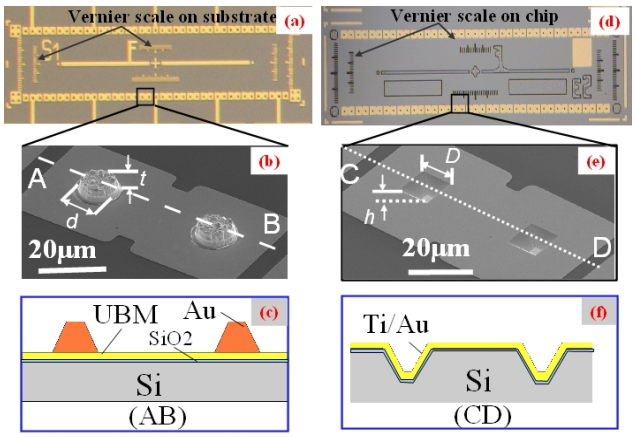

Fig. 3 Fabricated substrate (left) and chip (right) samples. Zoom-in images show the Au bump (b) and Au-deposited hollow pyramid (e). d = 10 μm, t = 6 μm; D = 12 μm, h = 4 μm. (c), (f) are the sketch of cross-section views of these elements.

For examining the bonding approach, chips and substrate with dimensions of 500 µm × 2000 µm × 380 µm and 10000 µm × 10000 µm × 380 µm (width × length × thickness) were fabricated, i.e. with bumps on substrate and hallows on chip. Also for testing purpose, chips were fabricated from IR-transpairent material (i.e. silicon) and micro-vernier structures with the finest resolution of 100 nm were also created (during the processes to create bump and hollow bonding pad) at the bonding interface for the assessment of the bonding alignment accuracy.

Fig.3 shows the hollow cavities fabricated on the chip and the truncated cone bumps fabricated on the substrate. Gold pads with hollow cavities were micro machined on silicon wafers using wet anisotropic (TMAH) etching and electron beam physical vapor deposition (EB-PVD) processes, respectively. Au bumps were evaporated using EB-PVD. The total number of truncated cone bump-hollow concave pairs is 80.

3. Experimental results and discussion

The bonding process was implemented using a ultrasonic-enhanced flip chip bonding machine (i.e. Bondtech Co., Ltd., CA-300) with alignment accuracy in the range of 2 µm. In this work, ultrasonic-enhanced flip-chip bonding, which utilizes ultrasonic energy along with the thermal energy to generate inter chip-connection, was utilized to apply bonding treatments to create strong joints. By this advanced technology, we can achieves eventually to lower the processing temperature and pressure compared with the conventional thermocompression bonding process [4].

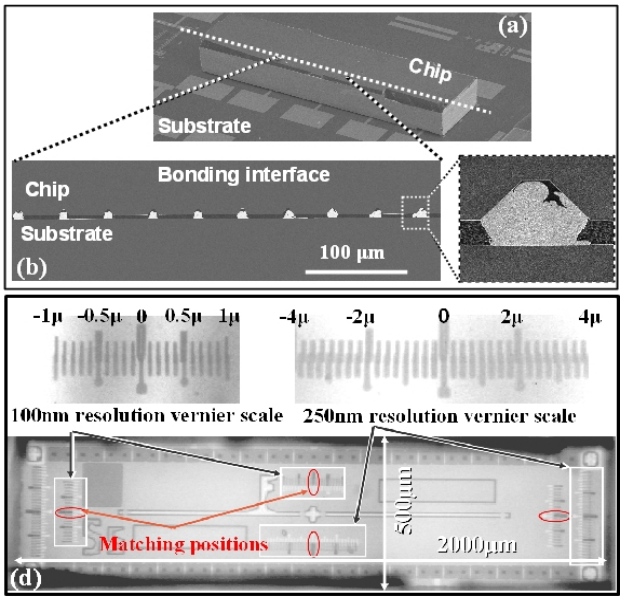

Fig. 4 Images of a typical bonded chip. Force of 15 N, along with ultrasonic energy of 48.5 kHz wave, amplitude of 2.2 µm activated in 500 ms, were applied at ambient temperature. (a) is the bird's-eye view of the chip on substrate; (b) is the cross-section view at bonding interface; (c) is the IR images showing the micro vernier, illustrating the bonding tolerance, confirming the self-correction function of truncated cone bump and hollow concave structures after bonding process.

The chip bonded on the substrate is shown in Fig.4(a). Fig.4(b) and (c) illustrate the cross-section view at bonding interface. Bonding accuracy is confirmed using the mentioned micro vernier scale. Fig.4(d) is the infrared (IR) images through a chip after alignment and bonding processes. The top chip was aligned with bottom chip under the assistance of bump and hollow pair structures, resulting in high-precision aligned bonding, i.e. less than 100 nm (that is the resolution of the fabricated vernier scale) in transverse offsets. The bonding process time was the same as normal bonding (i.e. without using of alignment self-correction structures) and consequently shorter to compare with other bonding approach owning equivalent bonding accuracy [3].

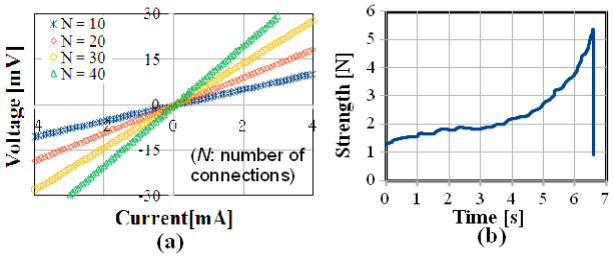

Fig. 5 I-V characteristic of the bonding interconnection (a), and shear bond strength test result (b).

Moreover, with the proposed interconnection, the contact area became larger, i.e. increasing approximately 30% in this case, to compare with conventional (flat) bonding pad, resulting in lower contact resistance and higher share strength. Electrical performance and shear strength of bonded joints were also characterized (Fig.5). The linearity of I-V characteristics confirmed the perfect Ohmic contact of the interconnections. Shear bond strength of 5.3 N was observed.

4. Conclusions

A new advanced bonding approach has been introduced. By efficiently modifying the bonding bump and pad structures of the flip-chip bonding process, significant improvement was achieved in terms of alignment accuracy and process time-efficiency. We confirmed successfully that misalignment in the alignment process (normally in alignment accuracy of the range of 2 µm) was self-corrected by this new bonding approach.

Although experiments for optimizing the bonding approach, such as hallow shape, dimensions, as well as bonding parameters, should be implemented, the initial incurred results indicate that this approach is quite promising to achieve practically high precision alignment in electronics-optics heterogeneous integration applications.

Acknowledgments

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