

Optoelectronic Heterogeneous Integration Technology Using Reductant-Assisted Self-Assembly with Cu/Sn Microbump

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1. Introduction

Heterogeneous integration has attracted much attention to realize high-performance system. 3D integration technology which vertically stacks large-scale integration (LSI) is a promising integration method owing to its high-speed data transmission and low-power consumption [1]. In addition, optical interconnection with vertical cavity surface-emitting laser diode (VCSEL) and photodiode (PD) have much potential applications [2]. Figure 1 shows concept of this work. In heterogeneous system integration, multi and tiny components must be massively assembled with high precision and in high throughput. Robotic pick and place methods currently contribute to high-end packaging processes, however, one-by-one sequential methods have a serious tradeoff problem between assembly throughput and alignment accuracy.

Self-assembly methods by water-based droplets in the atmosphere are attractive solutions to precisely handle multi and tiny components using water's high surface tension. We have successfully demonstrated that dies with In/Au microbumps are flip-chip bonded on wafers by self-assembly with pure water [3]-[5]. This paper deals with flip-chip self-assembly of dies with Cu/Sn microbumps. Sn-based solders are popular in 3D integration researches due to their high reliability and low cost. Sn solders are sensitive to oxidation, and thus, we employed water-soluble flux as liquid for chip self-assembly. Flux is essential for electronic packaging acts as reductant agents and plays a crucial role to remove oxide layers. In this paper, self-assembly with such functional liquid is demonstrated using VCSEL-like dies with Cu/Sn microbumps. This paper also describes the electrical characteristic of the resulting Cu/Sn microbump daisy chains.

2. Experimental

The fabrication processes for substrates with Cu/Sn microbump and 3-mm-square chips with Ni/Au pads are shown in Fig. 2. Firstly, 2- μm -thick Cu wirings and 3- μm -thick bumps were patterned on a thermally oxidized wafer with sputtered Ta barrier and Cu seed layers by lithography and electroplating. After removal of the sputtered Ta and Cu, a hydrophilic tetraethylorthosilicate (TEOS) oxide for bonding area were deposited by plasma-enhanced chemical vapor deposition on Cu covered with sputtered SiO₂. Then, contact holes were fabricated by reactive ion etching (RIE). After another lithography pro-

cess, 6- μm -thick Sn was deposited, followed by a lift-off. Finally, thin hydrophobic fluorocarbon layer was formed outside the bonding areas by another lift-off to give the bonding area with a side length of 2.975 mm defined by photolithography. In the fabrication process of chips, electroplating for Cu microbumps is followed by Ni barrier and Au contact deposition and lift-off. After TEOS oxide deposition, contact holes and 2.975-mm square bonding areas were defined by lithography and RIE. Finally, the approximately 3-mm-square chips were obtained by mechanical dicing. Figure 3 shows self-assembly processes. A droplet (approximately 0.4 μl) of ultrapure water or water-soluble flux as self-assembly liquid was supplied onto the bonding area. The chip was released bonding-side down onto the droplet using a vacuum tweezer, and was precisely self-aligned to the bonding area by liquid surface tension. After spontaneous evaporation of liquid, microbumps between self-aligned chips and the corresponding substrate were bonded with thermal compression. The bonding conditions are as follows: bonding load of 90 N/chip, bonding temperature of 200°C, and heating time of 4 min.

3. Results and Discussion

Figure 4 shows top view of bonding side of the resulting chip and substrate having 2.975-mm-square bonding areas. The chip and the substrate were interconnected each other by a peripheral daisy chain consisting of Cu/Sn microbumps (70 μm in a side length /125 μm in pitch) and wires (20 μm in width).

Figure 5 shows results of contact angle measurement on the hydrophilic and the hydrophobic areas, using ultrapure water or water-soluble flux respectively. Compared with contact angles of water, flux showed small contact angle in both areas because some additives in flux decrease surface tension of water. By using flux, however, chips can be precisely self-aligned to substrates due to 40-degree wettability contrast between the hydrophilic and hydrophobic areas. Also, a flux droplet was confined in a hydrophilic area without seeping outside.

Chips were self-aligned to the bonding areas by using both water and flux, which was similar to our previous work [5]. However, immediately after thermal compression, chips self-aligned with water were displaced outside the bonding area. On the other hand, chips self-aligned with flux were strongly bonded in the bonding areas. An *I-V*

characteristic of a daisy chain using self-alignment with flux was measured as shown in Fig. 6. The contact resistance of the resulting daisy chain interconnection via all 88 microbumps could be obtained without disconnection, and contact resistance per a bump was estimated to be approximately 24 mΩ.

Figure 7 shows a scanning electron microscopy (SEM) cross-sectional image of a bonding interface between an Ni/Au pad and a Cu/Sn microbump after thermal compression. As seen from Fig. 7, alignment error was estimated to be approximately 1.9 μm. This alignment accuracy would attribute to mask alignment error derived from photolithography processes to define the bonding areas.

4. Conclusions

We demonstrated self-assembly of chips onto substrates with Cu/Sn bumps using water-soluble flux having reducing function to SnO. The chips were successfully self-assembled within 2 μm in alignment accuracy. Also the chip was strongly bonded to the substrate, and its interconnection through a peripheral daisy chain was confirmed without disconnection.

References

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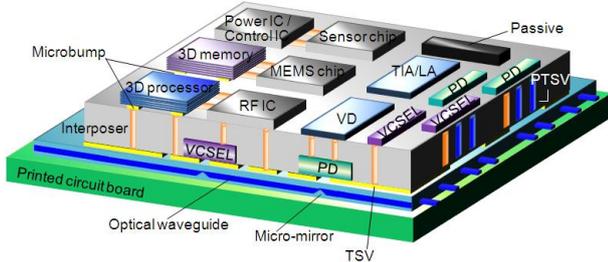


Fig. 1 Conceptual image of optoelectronic heterogeneous system with 2D/3D LSI, optics, and MEMS.

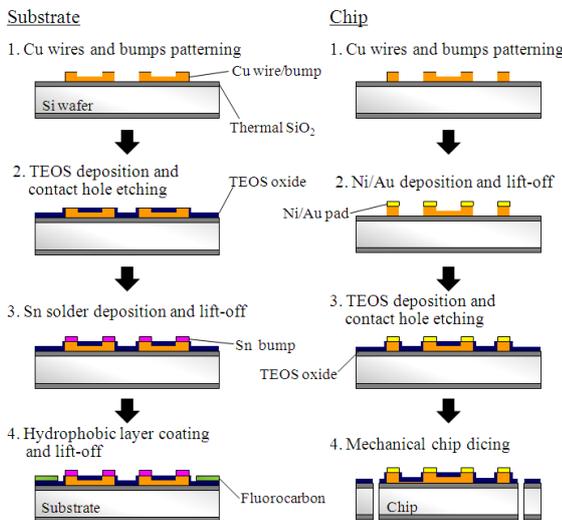


Fig. 2 Fabrication process for a substrate (left) and chips (right) for self-assembly.

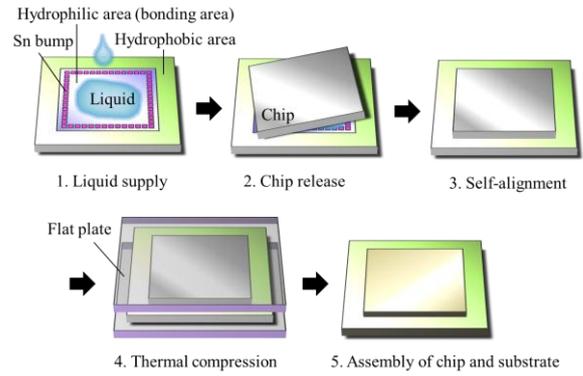


Fig. 3 Chip self-assembly onto substrate with Cu/Sn microbump.

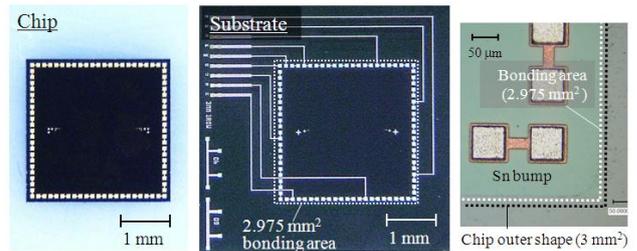


Fig. 4 Top views of bonding side of a fabricated chip (left) and a substrate with a bonding area (middle), and its magnified view (right).

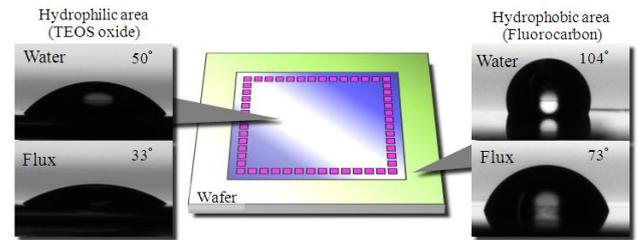


Fig. 5 Water and flux contact angle measurements on hydrophilic TEOS oxide and hydrophobic fluorocarbon.

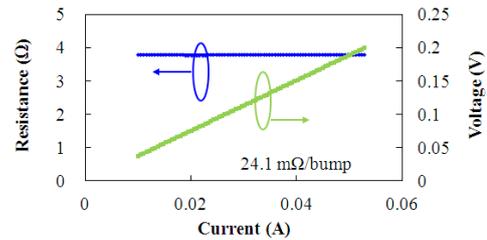


Fig. 6 I-V characteristics of microbump contact resistance measured using a daisy chain with Cu/Sn microbump chain by self-assembly.

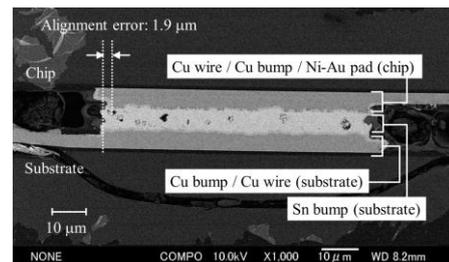


Fig. 7 SEM cross-section of a bonding interface between Ni/Au pad and Cu/Sn microbump on a self-assembled chip with functional liquid of flux.