

## 3D Integration with Wafer-to-Wafer Bonding

W. C. Lo<sup>1#</sup>, C. T. Ko<sup>1,2</sup>, and K. N. Chen<sup>2</sup>

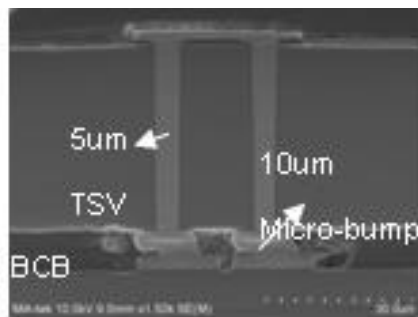
<sup>1</sup>Electronics and Optoelectronics Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan

<sup>2</sup>Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan

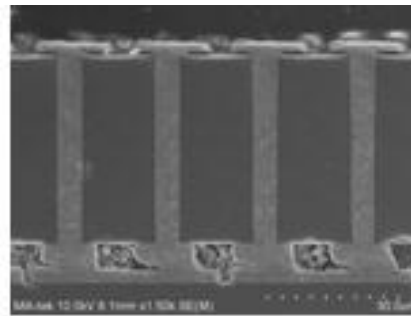
<sup>#</sup>Tel: 886-3-5917024, Fax: 886-3-5917193, Email: [lo@itri.org.tw](mailto:lo@itri.org.tw)

\* E-mail: JDKo@itri.org.tw, Tel: 886-3-5912336, Fax: 886-3-5917357

**Abstract** - 3D integration with TSV to form vertical interconnection shows the shortest wiring through multi-layers stacking. Wafer-to-wafer(W2W) stacking approach compared to others stacking methods(C2C or C2W) can provide the best throughput of stacking and lowest cost potentially in the future. W2W stacking consists of Metal-to-Metal direct bond, oxide-to-oxide direct bonding and hybrid bonding. The last one provide unique mass production-able wafer-level 3D integration scheme with Cu TSVs based on micro-joints and adhesive hybrid bonding, but previous two does not. Key techniques including TSV fabrication, micro-bumping, hybrid bonding, wafer thinning and backside RDL formation were well developed and integrated to perform the 3D integration scheme. A proposed test vehicle and study of structure design, process condition, electrical and reliability assessment of the wafer-level 3D integration scheme are demonstrated. The 3D integration scheme was assessed to be with excellent electrical performance and reliability, and is potentially to be applied for 3D IC applications.



Integrated stacked sample



5μm TSV daisy chain interconnect