Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp1183-1184

Electrostatic Temporary Bonding Technology and TSV Formation for Reconfigured Wafer-to-Wafer 3D Integration

Hideto Hashiguchi[1], Jichoel Bea[2], Yuki Ohara[1], Takafumi Fukushima[2], Kang-Wook Lee[2], Tetsu Tanaka[1, 3], and Mitsumasa Koyanagi[2]

[1] Dept. of Bioengineering and Robotics, Tohoku Univ.
6-6-01 Aza-Aoba, Aramaki, Aoba-ku, Sendai 980-8579, Japan
Phone: +81-22-795-6258, E-mail: link@lbc.mech.tohoku.ac.jp
[2] New Industry Creation Hatchery Center (NICHe), Tohoku Univ.
[3] Dept. of Biomedical Engineering, Tohoku Univ.

1. Introduction

To increase production throughput and yield in 3D chip stacking, we have developed a 3D integration technology based on reconfigured wafer-to-wafer alignment and bonding [1]-[3]. A reconfigured wafer consists of many KGDs (known good dies) and a carrier wafer on which the many KGDs for the 1st layer are assembled and temporarily bonded in chip-to-wafer stacking manner. The many KGDs on the reconfigured wafer are then transferred to another target LSI wafer in batch processing after wafer-level alignment and bonding to give 3D LSI wafers with the many KGDs. Finally, the 2nd and 3rd-layer KGDs are stacked in layers by repeating the chip assembly, temporary bonding, and chip transfer processes. Fig. 1 shows the conceptual schematic of reconfigured wafer-to-wafer 3D integration scenario.

The key technology of reconfigured wafer-to-wafer 3D integration is temporary bonding and debonding of KGDs. A number of research groups have reported temporary bonding/debonding technologies using high-heat resistant polymeric adhesives [4]. However, their debonding processes by thermomechanical release [5], solvent release [6], and laser ablation release [7] are complicated. In the present paper, we employ an electrostatic clamping force in order to temporarily bonding chips that are assembled onto an electrostatic carrier. We demonstrate via etching for TSV formation in a Si chip that is temporarily bonded on the electrostatic carrier, and then, transferred to another carrier wafer using a new reconfigured wafer technology.

2. Experimental

Fig. 2 shows a cross-sectional structure of an electrostatic Si carrier wafer used in this study. The electrostatic carriers were prepared by standard photolithography, CVD, and RIE techniques. First, B-doped p-type Si (100) wafers with a resistivity of 10-15 Ω•cm were thermally oxidized to form a 1-μm-thick SiO_2 layer on them. Then, an Al/W layer was deposited on the thermal oxide by sputtering. After pattering with a photoresist, Al/W electrodes were formed, and then, 6-μm-thick plasma-TEOS oxide was deposited on the electrodes, followed by contact etching. Si chips with a SiO_2 layer on their top surface are assembled on the electrostatic carriers. After that, high DC voltage 100 V or 200 V was applied between the chips and Al/W electrodes on the electrostatic carriers, as shown in Fig. 2.

Fig. 3 shows a process flow from chip assembly to deep Si etching for TSV formation through chip transfer from an electrostatic carrier to another glue carrier. We call these carriers "*Reconfigured Wafers*". First, 5-mm-square chips with a thickness of ~100 μm were assembled on the electrostatic carrier. After chip temporarily bonding by electrostatic force, the chips were mechanically or electrically debonded and then transferred to the corresponding glue carrier on which a 20-μm-thick thermally stable temporary adhesive was coated. The followings were photolithography processes with the chip-on-wafer structure. The chips were etched to give deep Si vias by ICP-RIE with SF_6 and C_4F_8 gases, followed by photoresist removal.

3. Results and discussion

Fig. 4 shows voltage loss depending on time and applied temperature. The voltage between chips and Al/W electrodes indicates electrostatic chip clamping force, which is expressed as the following equation:

$$F = \frac{A\varepsilon_0\varepsilon_r{}^2V^2}{2d^2} \quad ,$$

where F for clamping force, A for chip area, d for space/gap between the charges, ε_r for relative dielectric constant, and V for applied voltage. Therefore, the clamping force increase with an increase in surface voltage differences between the chips and electrodes. In addition, the electrodes formed on the carrier wafer hold the chips without the continuous presence of power supply. Compared with bipolar-type electrostatic carriers, unipolar-type ones are easy to design and to manufacture and realize higher clamping forces than the bipolar-type. As shown in Fig. 4(a), initial DC voltage (100 V or 200 V) dramatically decreases by half within 10 min when the chips are placed upside down on the electrostatic carrier, in short, the 100-nm-thick thermal oxide layer formed on the chips is not contacted to the P-TEOS layer on the electrostatic carrier. After 10 min later, the voltages are slightly decreased. In contrast, Fig. 4(b) shows that initial applied DC voltages (200 V) are kept constant at around 200 V over 15 min, indicating that the clamping force can be maintained continuously after applying DC voltages to the chips. Here, the thermal oxide layer formed on the chips is contacted to the P-TEOS oxide layer. The clamping force seems to be not affected by annealing temperatures at 100°C and 200°C after electrostatic temporary chip bonding, as shown in Fig. 4(b). However, the 100-μm-thick chips

that are placed on the carrier wafers in a oxide-up bonding manner can be transferred to glue carrier wafers with temporary adhesives. As shown in Fig. 5, Si deep vias with a diameter of 20 μm and a depth of approximately 30 μm are successfully formed in the transferred chip on the reconfigured wafer.

4. Conclusions

Si chips were able to be assembled and temporarily bonded on electrostatic carrier wafers and transferred to another glue carrier called "*Reconfigured Wafers*" with temporary adhesives. In addition, deep Si vias were successfully formed in the chips that would be transferred again to target wafers to give 3D stacked chips.

Acknowledgements

This research was supported by a Grant-in-Aid for Scientific Research "Grant-in-Aid for Scientific Research (S)", No. 21226009 from the Japan Society for the Promotion of Science.

References

[1] T. Fukushima et al., IEDM Tech. Dig., (2007) 985.
[2] T. Fukushima et al., IEDM Tech. Dig., (2009) 349.
[3] T. Fukushima et al., Proc. of ECTC, (2010) 1050.
[4] W. L. Tsai et al., Proc. ECTC (2011), 989.
[5] S. Pargfrieder et al., Proc. ECTC (2008), 1301.
[6] K. Tamura et al., Proc. ECTC (2010), 1239.
[7] T. Itabashi et al., Proc. ECTC (2010), 1877.

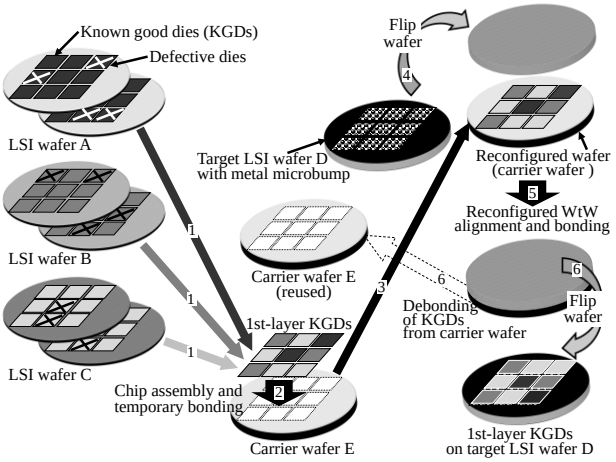

Fig. 1 A conceptual schematic of reconfigured wafer-to-wafer 3D integration.

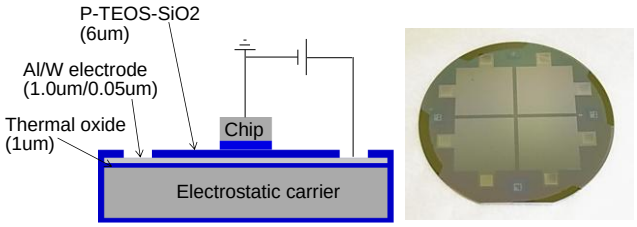

Fig. 2 High-voltage power supply system with unipolar-type electrostatic carrier (left) and photo of a proto-type electrostatic carrier (right).

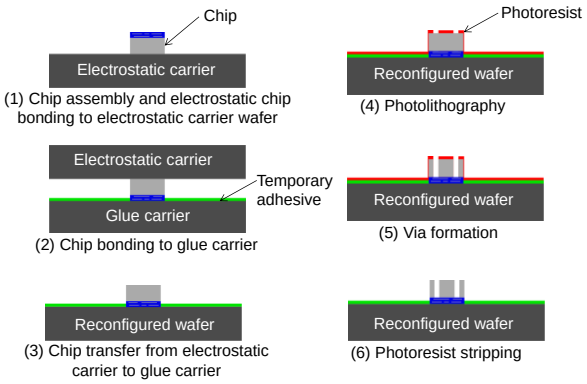

Fig. 3 A process flow of TSV formation on self-assembled chips temporarily bonded on an electrostatic carrier wafer.

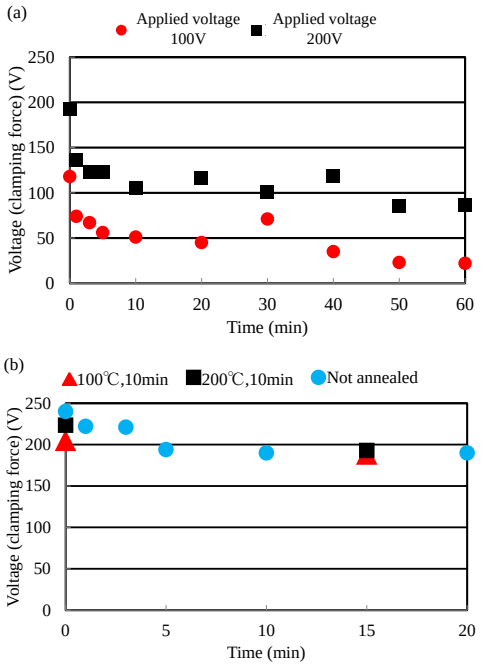

Fig. 4 Effect of initial applied voltage (a) and temperature (b) on surface voltage on chips temporarily bonded on electrostatic carrier wafers as a function of holding time.

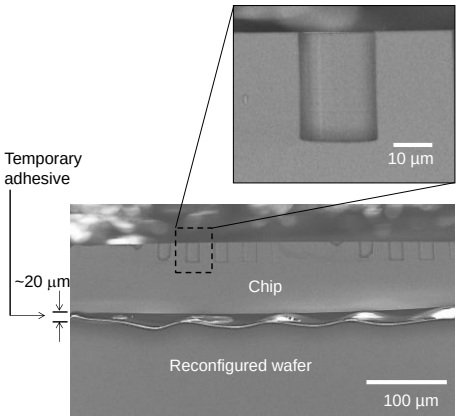

Fig. 5 Cross-sectional SEM images of Si vias formed on a chip transferred to a reconfigured wafer after temporarily bonding on an electrostatic carrier.