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Reliability Challenges in High-Density 3D-Integration

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1. *Introduction and Experiment*

3D (three dimensional) – integration of LSIs (large scale integrated chip) is one of the key enabling technology in realizing the low-cost, high-performance system on chip for rapidly advancing wide range of microelectronics applications; smaller and more powerful smartphones, etc. In general the 3D-integration process (fig. 1a) involves the following four key processes such as (i) die/wafer thinning (ii) metal-TSVs (though-silicon-via) formation, (iii) metal μ-bumping, and (iv) injection of an organic underfill into the interlayer gap. Both TSVs and μ-bumps are used for electrical interconnections, whereas the organic underfill is injected between the stacked LSI dies for mechanical rigidity. Ultra thinning the die/wafer down to less than 30 μm is a necessary process in 3D integration, as it allows the interconnect length to be reduced, thus allowing a high density of vertical stacking for the given footprint volume. On the contrary, this die/wafer thinning process either leaves the whole thin die/wafer under residual stress or eliminates the gettering layer for heavy metal atoms coming from BEOL process (Fig. 1b). We have already demonstrated that the Cu atom (via back metal contamination) diffuses into the active Si within 30 minutes even at 200 ℃[1]. The CTE (co-efficient of thermal expansion) for the metal (the CTE of Cu is $\sim17\times10^{-6}$/K) of the metal-filled TSVs and μ-bumps is much greater than the CTE of Si ($\sim2.6\times10^{-6}$/K). This large CTE difference is posing a risk of undesired thermo-mechanical stress generation in the active Si of thin LSIs with a potential adverse impact on device characteristics, yield, and reliability [1-5].

It is expected that potential adverse reliability problems arising due to the local deformation of the stacked die (caused by the CTE difference between the organic underfill and the Si) is even much worse than that of the deleterious effect arising from the CTE difference between the metal (of TSVs and μ-bumps) and the Si of the LSI die. This enhanced CTE difference causes different degree of local bending in the stacked die around the μ -bump region and in the μ-bump space region as shown in fig. 1(c). Apart from the thermo-mechanical stress due to TSVs, there is also possible for the metal of TSVs to diffuse into the active Si. Thus, it is important to select the TSV-metals which have close CTE values and relatively small diffusion co-efficient in Si. In line with this we have proposed hybrid-TSVs for high-density 3D-LSIs, where the W-TSV (which has relatively higher resistivity as compared to Cu-TSVs, but very close CTE value, 4.5×10^{-6}/K with Si) are used for signal lines and Cu-TSVs are employed in P/G (power/ground) lines, as shown in fig. 1d.

In this paper, we focus our attention on some of the most potent reliability issues such as thermo-mechanical stress in active Si caused by metal TSVs and μ-bumps, and the local deformation of stacked die after underfill curing. Apart from that the residual stress and sub-surface defects present in the ultrathin wafer stress relieved by CMP (chemical mechanical polishing), PE (plasma etching), UPG (ultra-poly grinding), PG (poly grinding), DP (dry polishing), and #2000 after back-grinding will also be discussed. The stress propagation in the vicinal Si close to the TSVs and the local mechanical stress created by the local bending of the stacked die around the μ-bumps were characterized by using micro-Raman spectroscopy (μRS) from the top surface of a TSV array which measures the stress in the x and y directions at the step interval of few hundreds of nm.

2. *Results and Discussion*

The 2D-stress mapping data obtained on the stress relieved surface of ultra thin wafers with 10 μm thickness revealed that irrespective of the type of stress relief method, the active surface of the wafers is under severe tensile stress of +35 to +40 MPa (fig. 2). It is that this tensile stress appeared on the active surface of Si is basically propagating from the back side of the wafers where the amount of tensile stress is nearly twice that of the front side. Among various stress relieved wafers examined for the residual stress at the back-ground surface after wafer thinning, the μ-Raman data revealed that there exists a compressive stress of -30 MPa and -75 MPa respectively for 50 μm thick DP and CMP samples; whereas in the case of 10 μm thick wafers, regardless of the stress relief process, both the CMP and DP wafers possessed around -100 MPa of tensile stress. The dry polishing method leaves behind either the polycrystalline Si

crystallites or amorphous Si at the back-ground surface, which is evidenced from the presence of dark spots in the EBSP image (Refer fig. 3).

Shown in Fig. 4(a) is the HRTEM image obtained on the back-ground surface of 50 μm-thick Si wafer, stress relieved by DP. It is clear that the defective Si crystal produced by the back grinding process is left behind even after the stress relief process. However for the similar thickness, such defects were not observed in the Si wafer stress relieved by CMP and PE. As formed sub-surface defects in the DP-stress relieved wafers could well act as a external getter sites for the heavy metal atoms that are originating from the back metal contaminants as shown in fig. 4(b). We were able to confirm that the deposited Cu atom gets accumulated in the defective Si after annealing at the temperature of 300 ℃ for 30 min.

The 2D thermo-mechanical stress in the active Si caused by an array of Cu-TSVs with 20 μm-width and 40 μm-pitch values is shown in fig. 5, and data were collected after annealing at 300 ℃ for 30 min. As can be seen in the optical image (fig. 5 (a)), the Cu of the TSV starts accumulating at the center of the TSV. Finally, it results into Cu extrusion after annealing at 400 ℃ by relaxing the stress to almost zero. The stress relaxation is a combination of plastic (at lower temperatures) and creep deformation (at the higher temperatures) which fully reduces the stress in the copper [6,7]. At 300 ℃, the via metal induces a compressive stress of -800 MPa circumferentially, and it decays exponentially into tensile stress and then to zero stress state (fig. 5 (c)).The FWHM of the Si Raman peak becomes larger for the compressive stress region (fig. 5 (b)).

Fig. 6 reveals the novel method to characterize the local mechanical stress originating from local deformation in the LSI die around μ-bump region, and the 2D-stress data is shown in fig. 7. It is worthy to note that the magnitude of locally induced mechanical stress and its propagation along the plane of the active Si due to local bending are relatively too high as compared to the thermo-mechanical stress induced by the metal-TSVs and μ–bumps. In the present case, the μ-bump array (where the bump size and bump spacing are 5 μm and 100 μm, respectively) introduces a maximum tensile stress of more than +1500 MPa in the active area of top die around the μ–bump region. On the other hand, a relatively less amount of compressive stress (< -500 MPa) is exerted on LSI in the bump space region. Such a large tensile around the μ–bump region is not only deteriorates the device performance, but also severely degrades the mechanical strength of the stacked die, by and large ends in die-cracking.

3. *Summary*

The sub-surface micro-structure of the stress relieved ultra-thin Si wafers after back grinding, thermo-mechanical stress induced by the hybrid-TSVs (W-TSV for signal line and Cu-TSV for P/G line) in the active Si, and the local mechanical stress in the stacked LSI caused by local bending around μ-bump region were investigated. Even though the stress relief process of CMP was found to be the best among all the stress relief processes investigated, the crystal quality deteriorates with the decrease in the die thickness. The sub-surface defects in the back-ground Si wafers (stress relieved by DP) acting as external getter sites for Cu was confirmed. As high as -800 MPa of compressive stress was induced by 20 μm-width Cu TSVs in the active Si of the LSI die, after annealing at 300 ℃ for 30 min. The local deformation of the stacked thin LSI die was found to cause adverse reliability problem, as the amount of locally induced mechanical stress and its propagation along the plane of the active Si were too high when compared to the thermo-mechanical stress induced by the metal-TSVs and μ–bumps.

References
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[4]J. Chen and I.De Wolf, Semicond.Sci.Technol. **18,** (2003) 261.
[5]J. Gambino *et al*, . SSDM Extd. Abs., pp.793 (2011).
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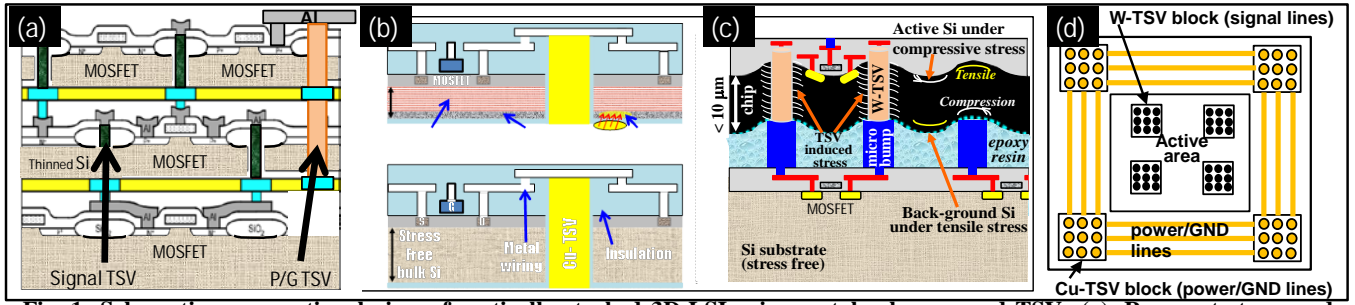[7]I.De Wolf,*et al,* Proc. ECTC, pp. 332 (2012).

Fig. 1: Schematic cross-sectional view of vertically stacked 3D-LSI using metal μ-bumps and TSVs (a), Remnant stress and defective Si (that may act as external getter site) present in the background surface of ultrathin LSI die (b), Thermo-mechanical stress induced by TSVs and μ-bumps and local deformation of the LSI around μ-bump region caused by organic underfill (c), and the proposed hybrid-TSV model (W and Cu-TSVs respectively for signal and P/G lines) for high-density 3D-LSI.
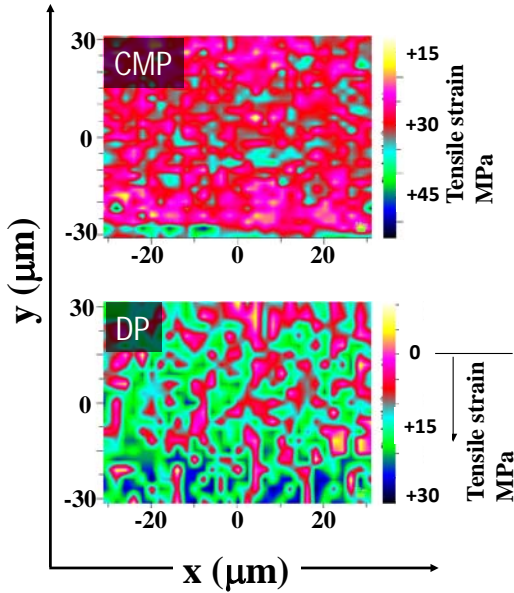

Fig. 2: 2D-stress mapping image obtained on 10 μm-thick LSI dies stress relieved by Chemical Mechanical Polishing, CMP (a), and Dry Polishing, DP (b).
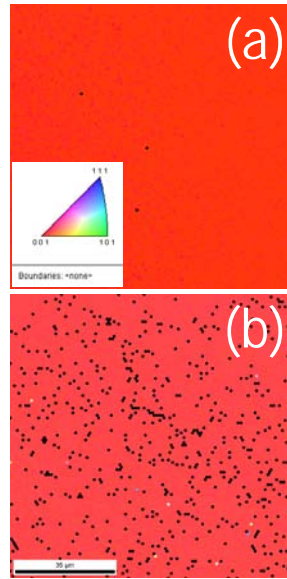

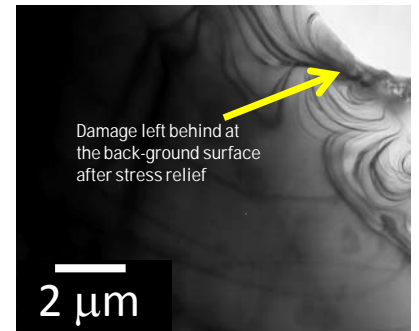Fig. 3: 2D-IPF image obtained for dry polished Si chips: (a) Top side and (b) bottom side.

Fig. 4(a): HRTEM image obtained over 50 μm-thick Si wafer stress relieved by dry polishing after back grinding
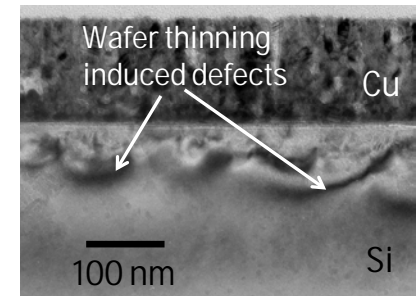

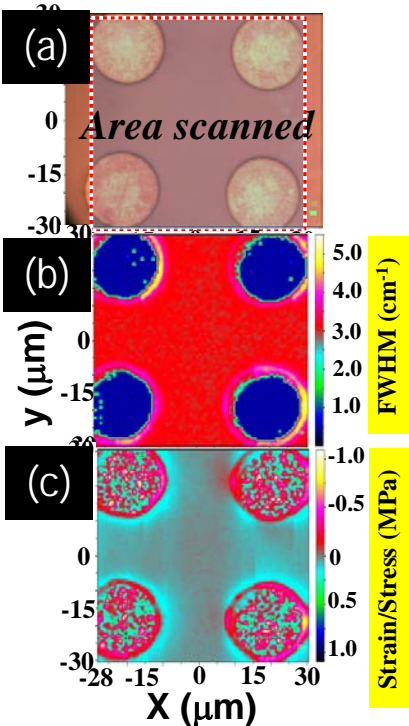Fig. 4(b): Gettering of Cu at defective Si produced at the stress relieved surface by DP.

Fig. 5: 2D-stress mapping data obtained for LSI chip containing Cu-TSVs with 20 mm diameter. (a) optical microscopic image, (b) FWHM of Si peak, and (c) stress distribution.

New Local Bending Method Using Si columnar array

(i) Formation of Si or CuSn microbump

(ii) Epoxy (for 3D-LSI use) resin coating

(iii) Bonding of 3D-LSI wafer/chip

(iv) Curing (160 ℃, 1h)

Device under stress/strain

Bonding parameters

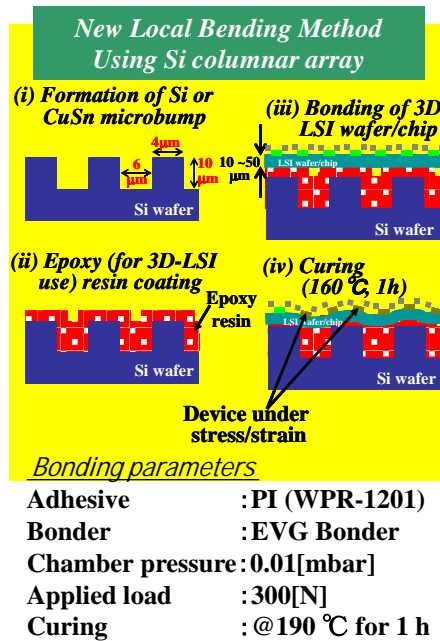|	
Adhesive	: PI (WPR-1201)
Bonder	: EVG Bonder
Chamber pressure	: 0.01[mbar]
Applied load	: 300[N]
Curing	: @190 ℃ for 1 h

Fig. 6: Novel method to evaluate the local mechanical stress in stacked 3D-LSIs caused by local deformation after organic underfill injection and curing.
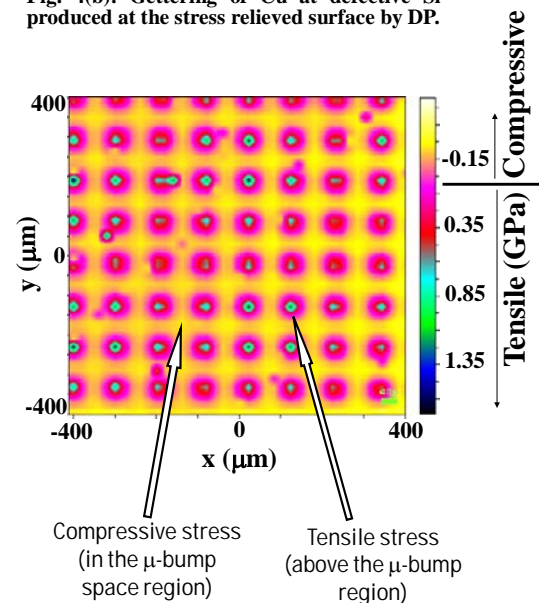

Fig. 7: 2D-stress distribution on the active Si surface of the stacked 3D-LSI die