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Dominant Structural Factors of Residual Stress Distribution in Stacked Silicon Chips Mounted in 3D Packages and Modules

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1. Introduction

Flip-chip structures using area-arrayed tiny metallic bumps such as Cu or Au are surrounded by insulating material (underfill) such as epoxy or plastic for assuring the reliability of the connection between an LSI chip and a substrate or another chip. Thus, the local distribution of the residual deformation and residual stress on a transistor formation surface of a chip appears and it is changed drastically by changing the interconnection structure of packages or modules from a wire-bonding structure to an area-arrayed flip-chip bonding structure. In some cases, a periodic stress with amplitude of more than 100 MPa appears due to the periodic alignment of metallic bumps because of the mismatch in the material properties such as the coefficient of elasticity and the thermal expansion coefficient between metallic bumps and underfill material even in a SOS (Silicon On Silicon) structure. [1]

Such large stress and strain should cause the change of electronic band structures of semiconductor and dielectric materials and thus, the electronic performance of devices changes drastically. [2] In addition, the reliability of interconnections should be degraded by stress-induced migration of component element in the interconnections. Delamination between copper thin-film interconnection and base material and the growth of voids and hillocks are often observed in various reports. Therefore, it is very important to minimize the local stress and strain in devices in order to assure the reliability of products. In this paper, the amplitude of the variation of the residuals stress in the three-dimensionally stacked silicon chips was analyzed using a three-dimensional finite element method as functions of the cross-sectional structure of the interconnection between the stacked chips and material properties of area-arrayed fine bumps. Also, the estimated residual stress was validated by stress-sensing test chips in which 2-μm long piezoresistance strain gauges were embedded.

2. Structural Analysis

Figure 1 shows an example of a three-dimensional finite element model for the stress analysis. Assuming the symmetry of the total structure, one fourth of the total structure was modeled for the structural analysis. Area arrayed bump alignment was assumed. The diameter and the height of Cu bumps were varied from 10 μm and 200 μm, respectively and the pitch of the bump was varied from 5 μm to 1000 μm. The width of the chip was assumed to 10 mm. A hexahedral solid mesh with 20-node was used for the analysis. The total numbers of nodes and elements were about 78,000 and 72,600, respectively. The chip was mounted on a silicon substrate with the electroplated tin/copper bumps at 150ºC. The thickness of the chip was varied from 280 μm to 50 μm. The materials constants used in the stress analysis are summarized in Table 1. Most materials were assumed to be elastic. Only Cu bumps were modeled as elastic-plastic material. Though silicon is anisotropic material, it was assumed to be isotropic material with Young's modulus of 167 GPa to simplify the analyses. This assumption may cause some error when the estimated results are compared with the experimental results.

Figure 2 shows an example of the distribution of the residual stress in a two-chip stacked structure. High tensile residual stress appears in TSV interconnections because of not only thermal stress but also intrinsic stress in the electroplated copper thin-films caused by densification of the film during annealing. In addition, periodic stress distribution appears in the stacked chip due to the periodic alignment of TSVs and bumps.

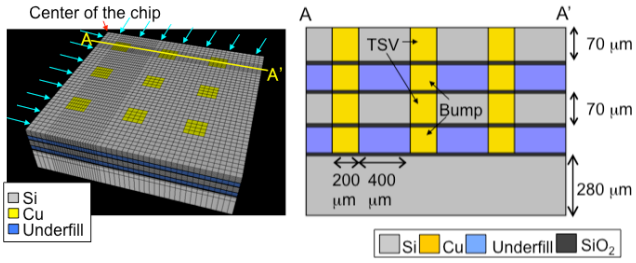


Fig. 1 Three-dimensional finite element model for analysis of residual stress and strain

Table 1 Materials constant

Material	Young's modulus (GPa)	Poisson's ratio	Thermal expansion coefficient (10^{-6}/K)
Si	167	0.07	3.0
Cu bump	117	0.3	17
Substrate	167	0.07	3.0
Underfill			15
(0 wt.%)	2.4	0.3	57
(40 wt.%)	5.1	0.3	39
(65 wt.%)	7.3	0.3	24

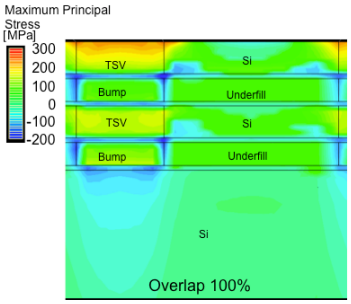


Fig. 2 Example of the estimated cross-sectional stress distribution of a silicon chip mounted on the area-arrayed bumps

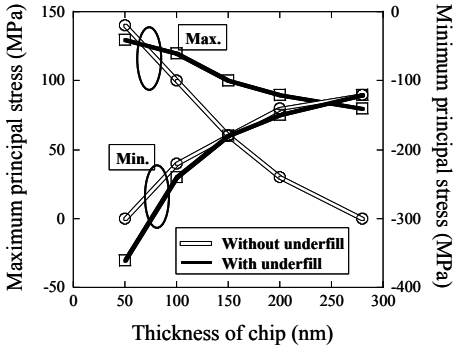


Fig. 3 Effect of underfill layer around Cu-bumps on residual principal stresses in silicon chip

The amplitude of the periodic stress varies drastically depending on the structure the 3D packages such as the thickness of a chip, mechanical properties of underfill, and the pitch of TSVs and bumps as shown in Fig. 3.

2. Experimental validation

The estimated results were validated by test chips. The local distribution of the residual stress was measured by using stress sensing chips in which the piezoresistive strain gauges were embedded Similarly, the amplitude of the local deformation of the stacked chip varies drastically as shown in Fig. 4. Clear periodic stress distribution appeared on each chip. However, the amplitude of the residual stress in each chip varied drastically as functions of structures and the combinations of materials used in the structures. At the same time, the amplitude of the local deformation of the stacked chips varied drastically as shown in Fig. 5. In this example, the amplitude varied from 100 nm to 3 mm as functions of bump pitch and materials constant of underfill. These measured values agreed well with the estimated results. Figure 6 shows the degradation of the crystallinity of copper interconnections in TSVs. In this example, a lot of voids appeared in the interconnection after the annealing at 400ºC due to stress-induced migration of the interconnections. The degradation rate was a strong function of their electroplating conditions such as current density and base material under the interconnections.

Therefore, it is very important to optimize both the structure of the stacked structure and fabrication process to assure the reliability of products.

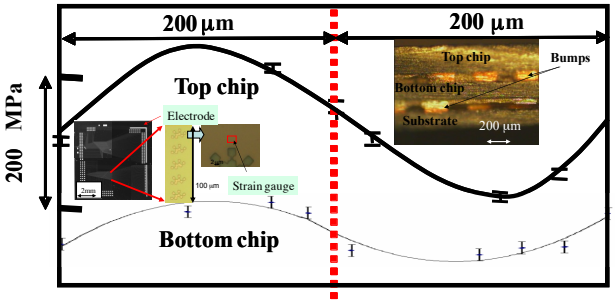


Fig. 4 Variation of the distribution of the residual stress between two bumps in a silicon chip mounted on area-arrayed fine bumps

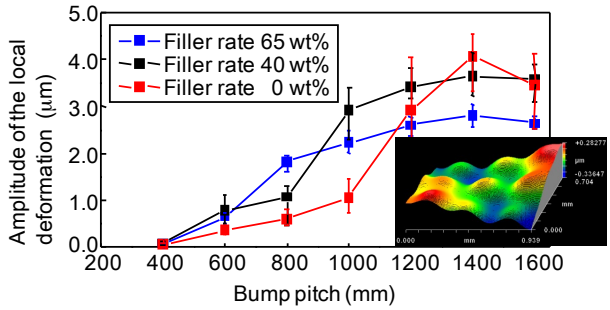
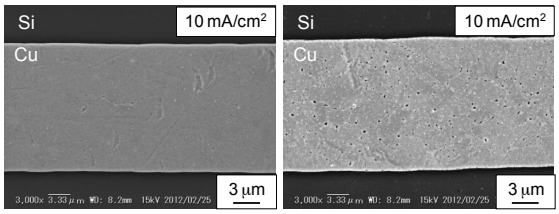


Fig. 5 Effect of bump pitch and mechanical properties of underfill on the local deformation of a silicon chip



(a) Just after annealing (b) 2 weeks after annealing

Fig. 6 Void growth in TSV interconnection due to stress-induced migration after annealing at 400ºC

3. Conclusions

The dominant structural factors of the local deformation and residual stress of a silicon chip were investigated quantitatively based on the results of three-dimensional finite element analysis and measurements of the local deformation and residual stress of the chip mounted on area-arrayed metallic bumps.

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