Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp1189-1190

# TSV Scaling with Constant Liner Thickness and the Related Implications on Thermo-mechanical Stress, Capacitance, and Leakage Current

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## ABSTRACT

TSV scaling with a constant liner thickness is studied in the context of 3D IC performance and reliability. TSV scaling is beneficial as smaller electrical parasitic such as capacitance and leakage current is obtained with smaller surface area. The thermo-mechanical stress improves significantly when TSV diameter is scaled from 9 μm (-243.3 MPa) to 5 μm (-50.5 MPa). However, TSV scaling results in rapid increase in the resistance and this must be properly addressed.

## INTRODUCTION

Through silicon via (TSV) has emerged as an essential enabler for the next generation of integrated circuits and systems for continuous performance growth ("More Moore") and functional diversification ("More than Moore"). TSV is commonly fabricated by high aspect ratio deep silicon etching, lining with dielectric for electrical isolation and super-conformal filing with copper [1] hence forming a metal-oxide-semiconductor (MOS) structure [2]. Integration of TSV poses new challenges. Due to large CTE mismatch between Si and Cu, large compressive stress is induced in the Si which causes mobility variation [3] or mechanical deformation [4]. TSV has strong electrical coupling with the doped Si substrate through the MOS structure. TSV parasitic capacitance has the most predominant impact on the circuit operation [5]. It is therefore imperative to control the electrical parasitic and stress for successful TSV integration. In this work, TSV scaling with a constant liner thickness and the implications on TSV stress, capacitance and leakage current are discussed beyond density improvement.

## EXPERIMENTAL

TSV ($\phi$ = 5, 7, 9 μm) with a depth of 10 μm are fabricated on 8" *p*-Si wafer. This aspect ratio is chosen for ease of fabrication and is sufficient to study the properties of the TSV. TSV is etched by using a BOSCH process in a deep reactive ion etcher (DRIE) using oxide hard mask. The liner (~200 nm) is deposited in a plasma-enhanced CVD chamber at temperature <400$^{o}$C using TEOS precursor. Subsequently Ta barrier and Cu seed are sputtered followed by super-conformal Cu ECP filling. Upon annealing (200$^{o}$C, 30min, $N_2$), the Cu overburden is then removed by CMP. Raman spectroscopy is used to investigate the stress level in the surrounding Si. Finally, contact holes are opened on oxide layer and Al is deposited and patterned to form contact pads for electrical probing. The process flow is summarised in Fig. 1.

## RESULTS AND DISSCUSSION

*Structure Fabrication*

In order to achieve a robust TSV, sidewall scallop roughness and oxide hard-mask undercut must be minimized to ensure void-free and conformal Cu filling. As evidenced from Fig. 2, the use of a dual-mask process and the addition of a small quantity of $C_4F_8$ during etching cycle improve both roughness and undercut significantly. In Fig. 3, TSV with PE-TEOS liner is fabricated with conformal step coverage. No void or delamination is observed in the Cu core after filling.

*Stress Measurement and Modelling*

Fig. 4 is a collection of Raman spectra along a TSV row of 5 μm diameter and 15 μm pitch. The Raman shift originated from the Si-Si peak is then translated into biaxial stress as presented in Fig. 5. Fig. 6 is comparison of biaxial stress (compressive) in Si surrounding the TSV with diameter of 5, 7 and 9 μm. It can be concluded the as TSV is scaled to smaller diameter, the stress level is reduced significantly due to smaller Cu volume. This is also predicted from finite-element analysis in Fig. 7 for a thermal load of 200 to 25 $^{o}$C.

*Electrical Measurement*

Since individual TSV has extremely small capacitance and leakage current, TSV array as shown in Fig. 3(c) is used for measurement in order to minimize the measurement noise. The parasitic pad value is de-embedded during analysis. Fig. 8 shows the measured *CV* curves at 100 kHz at an average liner thickness of ~200nm. The capacitance changes from accumulation to depletion as the bias voltage increases demonstrating typical *p*-Si behaviour. *CV* curve of PE-TEOS liner shows a negative shift in the flat-band voltage ($V_{FB}$) due to the presence of positive fixed charge ($+Q_f$). The fixed charge density is estimated to be on the order of ~$1.8 \times 10^{12}$ $cm^{-2}$. As TSV is scaled, smaller effective surface area results in a reduction in TSV capacitance as seen in Fig. 9. The TSV length is fixed at 50 μm and this is a reasonable assumption due to challenges in wafer thinning and handling. The reduction in capacitance is beneficial for power consumption ($CV^2$). However, smaller TSV diameter results in rapid increase in the resistance which is detrimental for *RC* delay.

*IV* measurement is performed to evaluate the leakage of the liner. Fig. 10 shows that there is no abrupt breakdown up to at least 3MV/cm. Leakage current resistance is improved by a 300$^{o}$C annealing for 30 min in forming gas ($N_2/H_2$) or nitrogen gas ($N_2$) as summarized in Fig 11. Post annealing, the leakage current at mid-distribution at an electric field of 2MV/cm is improved by ~10× which is comparable with value reported in [6]. The leakage current in the TSV is expected to be smaller when it is scaled at constant liner thickness (Fig. 12) as the effective area is reduced.

## CONCLUSION

It is shown that TSV scaling with constant liner thickness is beneficial for thermo-mechanical stress, capacitance and leakage current control. However, increase in resistance must be carefully controlled for overall performance of 3D IC.

## REFERENCES

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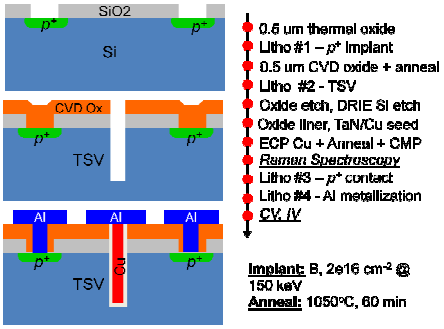


**Fig. 1** Process flow for TSV test structures fabrication. The structures include a Cu core as the gate, PETEOS liner, and a *p*+ contact as ground.

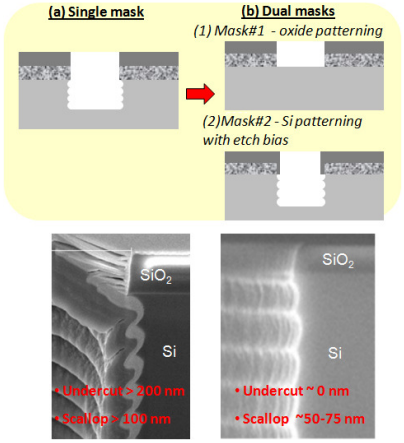


**Fig. 2** A dual mask process and proper passivation are used to improve the overall undercut and scallop roughness in the TSV.

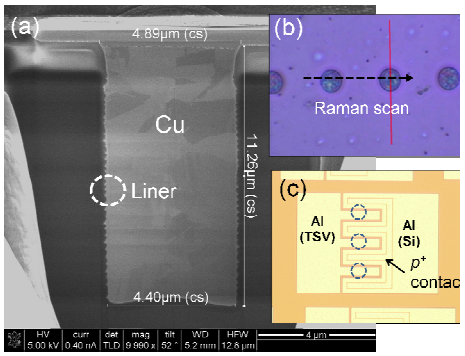


**Fig. 3** (a) TSV with Cu as the core conductor and PE-TEOS liner shell for electrical isolation. The diameter is ~5 µm and the depth is ~10 µm. Conformal deposition of liner is achieved using PECVD. (b) Raman scan along TSV row. (c) Electrical structure for *CV* and *IV* measurement.

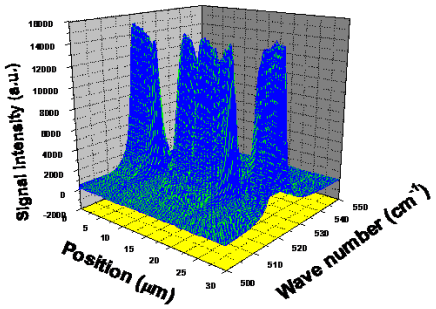


**Fig. 4** Raw data from Raman spectroscopy (laser wavelength = 442 nm) along TSV row as shown in Fig. 3(b). The wave-number is taken between 500 to 550 $cm^{-1}$.

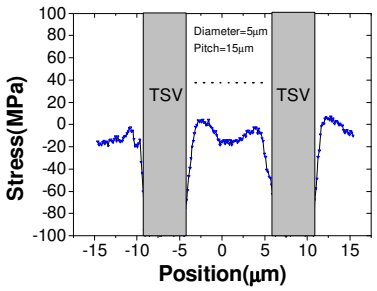


**Fig. 5** Variation of Si stress along TSV row as estimated from Raman shift in Fig. 4.

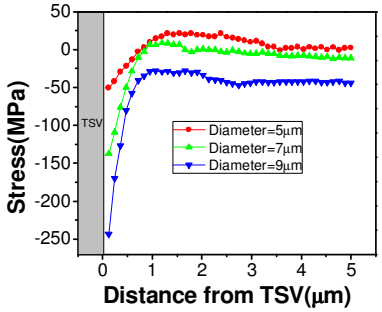


**Fig. 6** Comparison of Cu-TSV stress on the surrounding Si as measured from Raman spectroscopy. TSV scaling is beneficial for stress reduction.

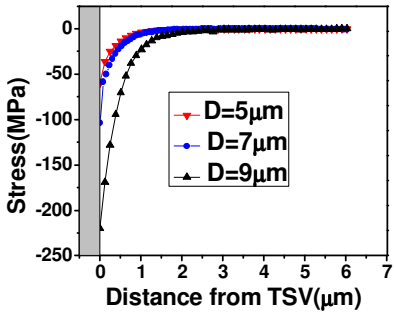


**Fig. 7** Stress induced in the surrounding Si by Cu-TSV as predicted by finite-element analysis. Material properties for Cu, $SiO_2$, and Si are: $E$ = 120, 70, 170 GPa, $CTE$ = 16.5, 0.5, 2.6 ppm/K, $\nu$ = 0.34, 0.17, 0.28.

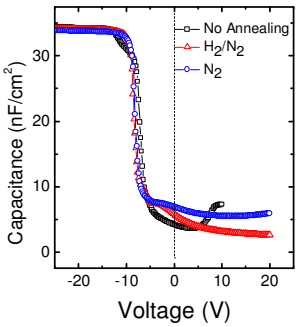


**Fig. 8** Summary of *CV* characteristic of PETEOS liner with various annealing ambient. $Q_f$ is ~ $9.7x10^{11}$ $cm^{-2}$ and $V_{FB}$= -9.4V ($H_2/N_2$).

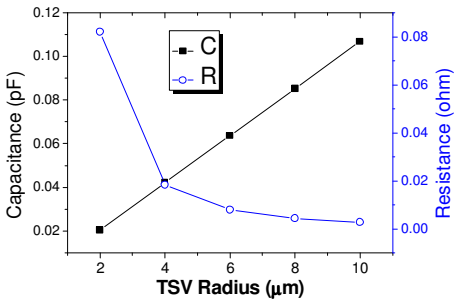


**Fig. 9** Scaling of capacitance and *RC* product with TSV radius. TSV length is fixed at 50 µm. While TSV scaling benefits the capacitance, resistance shows a reverse scaling behavior.

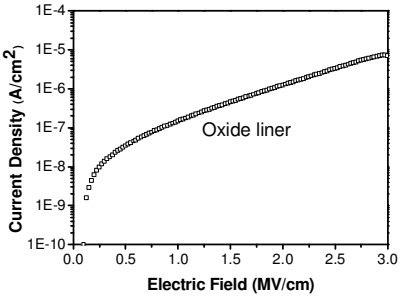


**Fig. 10** *I-V* characteristic of TSV-MOS.

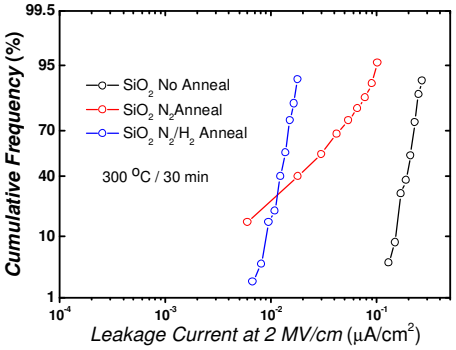


**Fig. 11** Summary of leakage current PETEOS liner. Annealing in $N_2$ and $N_2/H_2$ (300 °C, 30 min) is effective in suppressing the leakage current.

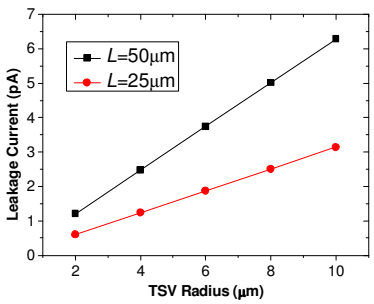


**Fig. 12** Leakage current variation with TSV scaling for TSV length $L$ of 50 and 25 µm.