Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp1191-1192

Racetrack Memory 2.0: a high performance, current controlled, domain-wall shift-register storage-class memory

Stuart S.P. Parkin[1]

[1] IBM Almaden Research Center
650 Harry Road, San Jose, CA 95120, U.S.A.
Phone: +1 408 927 2390; E-mail: stuart.parkin@us.ibm.com

1. Introduction

The development of novel, high-performance, solid-state non-volatile memories is of considerable interest for improving the performance of main-stream computing and storage systems and for pervasive mobile computing applications. In recent years there has been considerable progress in the development of non-volatile memories that use the direction of magnetization of magnetic nano-elements to store digital information. Most research and development programs have focused on magnetic random access memories (MRAM) that use a magnetic tunnel junction (MTJ) as the magnetic storage element [1; 2]. The magnetic tunnel junction is composed of two thin magnetic layers separated by an ultra-thin layer of crystalline MgO through which spin-polarized tunneling currents flow [2; 3]. The conductance of the junction depends on the relative orientation of the direction of magnetization of the magnetic layers or electrodes. Large changes in conductance, corresponding to giant values of tunneling magnetoresistance, have been demonstrated using MgO tunnel barriers in combination with CoFe or CoFeB electrodes [3]. The direction of magnetization of the "storage" electrode sets the state of the memory. The other electrode, whose magnetization direction is usually unchanged during the operation of the memory, acts as the reference layer. The direction of the storage layer moment can be changed and set by passing a sufficiently large spin polarized current through the device by using the spin-angular momentum of the tunneling electrons. These deliver a spin torque to the magnetic moments in the storage later. The use of perpendicularly magnetized electrodes allows for the switching of the storage layer at much lower writing currents than is possible using in-plane magnetized electrodes [4; 5]. The challenge for spin-torque tunneling MRAM (STT-MRAM) is to develop MTJ structures which allow for writing of the storage electrode at sufficiently low currents that these can be provided by a minimum-size transistor to which the MTJ is connected, yet at the same time, provide sufficient stability of the magnetization direction of the storage electrode against thermal fluctuations. In addition, tight distributions of the currents required for writing and reading MTJs in dense arrays are needed so that reading and writing processes are completely independent of each other.

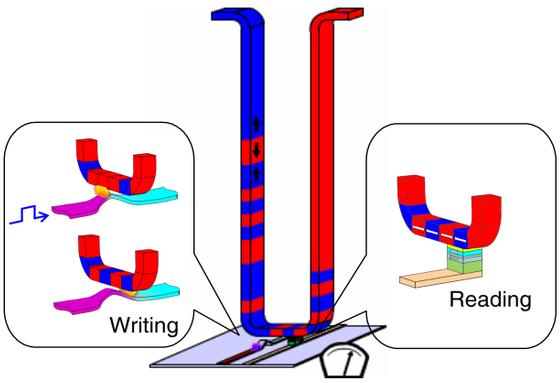

Figure 1. Schematic diagram of the vertical RM device including a U-shaped vertical magnetic nanowire in which magnetic domain walls (DWs) are injected and moved by nano-second long pulses of current. Data is stored either as the direction of magnetization of the domains or as the presence or absence of the DW between successive magnetic regions. Each racetrack has a single reading device composed of a magnetic tunnel junction (MTJ) sensor. The racetrack can either form one magnetic electrode of the MTJ sensor or the MTJ sensor can be remote from the racetrack and can detect the DWs by their fringing magnetic fields. DWs can be written by several means e.g Oersted fields from currents passed through a write line, fringing fields from a DW writing element or spin transfer torque [8].

2. Racetrack Memory

Racetrack Memory is a magnetic memory that conceptually is entirely distinct from MRAM [6; 7]. Data is stored as the presence or absence of magnetic domain walls in magnetic nano-wires. Racetrack Memory uses STT from spin-polarized currents to move a series of domain walls in lock-step at high speed along magnetic nano-wires. The domain walls are moved or shifted along the nanowires using nanosecond long current pulses past a single reading element that is incorporated into the racetrack nano-wires and are written into the nano-wires at a single point along the racetrack. The nano-wires can be aligned parallel or perpendicular to the surface of the underlying silicon wafer on which the circuits needed to create, manipulate and detect the domain walls are built using standard CMOS technologies. Racetrack Memory (RM) promises a high-performance, non-volatile memory with very high density, resulting in a low-cost storage-class

memory that could rival FLASH memory and magnetic disk drives in cost, yet using lower energy for much higher performance and reliability [7; 8]

3. Racetrack Memory Prototype

A recent demonstration of a fully integrated first-generation horizontal RM with arrays of 256 racetracks will be discussed [9; 10]. Racetrack memory cells were integrated in the back end of line with circuits built using an IBM 90 nm CMOS technology on 250 mm diameter wafers. The Racetrack memory cells were fabricated from permalloy ($Ni_{80}Fe_{20}$) nanowires. These formed one of the magnetic electrodes of an integrated magnetic tunnel junction element that was used to read the domain walls injected into the nanowires using on-chip writing elements. Full read and write functionality was demonstrated although a small assist field was used to aid the movement of domain walls along the nano-wire racetracks.

4. Racetrack Memory 2.0

The RM prototype used in-plane magnetized nano-wires formed from permalloy. We will contrast the current induced motion of domain walls in such nano-wires with nanowires formed from oligatomic Co and Ni layers in which the magnetization is perpendicular to the plane of the nanowire. We demonstrate in the latter case an additional interface-induced DW driving force that can drive the domain walls in either the same direction as in permalloy (electron flow), or in the opposite direction, depending on subtle changes in the structure of the nanowire. Moreover, we show that this additional force can lead to very high domain wall velocities of up to almost 1 km/sec. The large out-of-plane magnetic anisotropy in the Co/Ni multilayered racetracks also leads to very narrow domain walls allowing them to be closely spaced, and so allowing for much higher RM storage capacities. The particular properties of perpendicularly magnetized racetracks are so advantageous that they will enable a new generation of Racetrack Memory, namely Racetrack Memory 2.0.

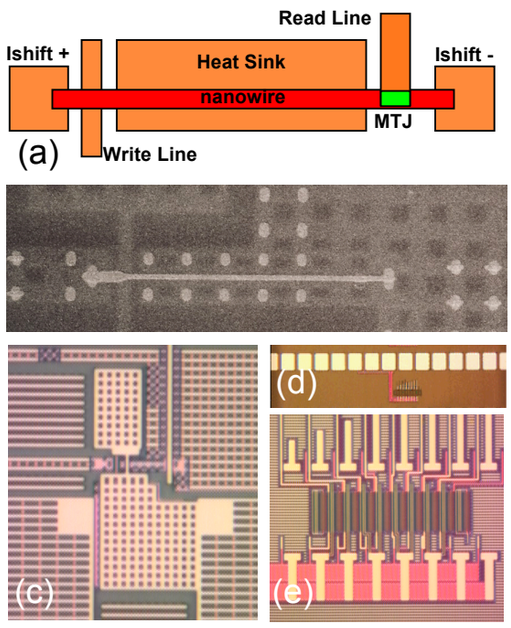

Figure 2. (a) Schematic diagram (top view) of a Racetrack Memory (RM) device. The nanowire forming the RM element in which magnetic domain walls are written and shifted along the nanowire is shown in red and is 12 μm long. The magnetic tunnel junction (MTJ) read element is shown in green and has a resistance of ~4 kΩ. Domain walls are written into the nanowire using current passed along the write line that is not in electrical contact with the nanowire. The electrical contacts for applying the domain wall shift currents are indicated as Ishift+ and Ishift- and connect to the ends of the nanowire through vias. (b) Scanning electron micrograph of an isolated RM cell (note that this image was taken before the top-level metal contact to the MTJ was fabricated); the nanowire here is; (c) optical image of an isolated RM cell; (d), (e) optical images of an array with 256 cells at low and high magnification. In (d), the horizontal array of contact pads is made up of 80 mm x 100 mm rectangular elements [9].

4. Conclusions

Racetrack Memory has made enormous progress since it was first proposed in 2002 [7]. The fundamental physics whereby spin polarized currents can move a series of domain walls along magnetic Racetracks has been demonstrated [11] and a first Racetrack Memory prototype built [9]. Recent developments in the current induced motion of domain walls in perpendicularly magnetized nanowires formed from ultrathin magnetic layers allow for the motion of closely packed, very narrow domain walls at high speeds. These developments auger second generation Racetrack Memory devices that have superior properties - namely high performance, low cost, low energy consumption and high reliability - than any other non-volatile memories currently under development.

Acknowledgements

I thank Kwang-Su Ryu, Luc Thomas, See-Hun Yang, Brian Hughes and Charles Retter at the IBM Almaden Research Center for their valuable contributions to this work as well as our colleagues at the IBM T.J. Watson Research Center and ITRI, Hsinchu, Taiwan for their help in building the first Racetrack Memory prototype.

References

[1] S.S.P. Parkin, et al., J. Appl. Phys. 85 (1999) 5828-5833.
[2] S.S.P. Parkin, Mater. Res. Soc. Bull. 31 (2006) 389-394.
[3] S.S.P. Parkin, C. Kaiser, A. Panchula, P. Rice, B. Hughes, M. Samant, S.-H. Yang, Nat. Mater. 3 (2004) 862-867.
[4] J.Z. Sun, Phys. Rev. B 62 (2000) 570-578.
[5] S. Ikeda, K. Miura, H. Yamamoto, K. Mizunuma, H.D. Gan, M. Endo, S. Kanai, J. Hayakawa, F. Matsukura, H. Ohno, Nat. Mater. 9 (2010) 721-724.
[6] S.S.P. Parkin, M. Hayashi, L. Thomas, Science 320 (2008) 190-194.
[7] S.S.P. Parkin, US6834005: Shiftable magnetic shift register and method of using the same IBM, USA, 2004.
[8] S.S.P. Parkin, Scientific American June (2009) 76-81.
[9] A.J. Annunziata, et al., Racetrack memory cell array with integrated magnetic tunnel junction readout, 2011, 24.3.1-24.3.4.
[10] L. Thomas, Y. See-Hun, R. Kwang-Su, B. Hughes, C. Rettner, W. Ding-Shuo, T. Ching-Hsiang, S. Kuei-Hung, S.S.P. Parkin, Racetrack Memory: A high-performance, low-cost, non-volatile memory based on magnetic domain walls, 2011, 24.2.1-24.2.4.
[11] M. Hayashi, L. Thomas, R. Moriya, C. Rettner, S.S.P. Parkin, Science 320 (2008) 209-211.