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Room-Temperature Detection of Spin-Accumulation Signals in a Silicon-Based MOSFET Structure with a Schottky-Tunnel Contact

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1. Introduction

The shrinking of silicon (Si)-based conventional complementary metal-oxide-semiconductor (CMOS) transistors will reach its intrinsic limits in the future. Because of this critical issue, spin-based electronic (spintronic) devices have been researched and developed intensively. To date, the experimental studies of novel techniques such as spin injection from ferromagnetic materials into nonmagnetic semiconductors have been reported on the basis of III-V semiconductor technologies [1,2]. To combine the spintronics with Si-based semiconductor industry, it will become important to explore Si-based spintronics from now on [3,4]. In particular, for ultra low power consumption, spin injection and detection technologies for Si without using an insulating tunnel barrier have been explored [5].

In this study, we demonstrate room-temperature spin injection into a Si channel in a metal-oxide-semiconductor field effect transistor (MOSFET) structure with a high-quality CoFe/n^+-Si Schottky-tunnel-barrier contact. By applying electric fields to the Si channel, the magnitude of the spin-accumulation signals can be modulated at room temperature. From the technological point of view, this study will lead to an acceleration of research and development of Si-based spin MOSFET with metallic source-drain electrodes [6].

2. Si-MOSFET structure with a CoFe contact

10-nm-thick $Co_{60}Fe_{40}$ epitaxial layers were grown on (111)-oriented silicon on insulator (SOI) by MBE at 60 ◦C [7], where thicknesses of the SOI and buried oxide (BOX) layers were ~75 and 200 nm, respectively, and the carrier density of the SOI layer was ~4.5×10^{15} cm^{-3} (1–5 Ωcm) at room temperature. The detailed growth procedures were reported in Ref. 7. An atomically flat interface between CoFe and Si was demonstrated even for the direct growth of ferromagnetic alloys on Si. Also, electron diffraction patterns near the interface showed no other crystal structure, indicating no influence of the silicidation reactions. For the three-terminal Hanle-effect measurements [4,8], an n^+-Si layer (Sb: 1×10^{19} cm^{-3}) was inserted between CoFe and SOI by a combination of the Si epitaxy using an MBE process with an Sb δ-doping technique. Conventional processes with electron-beam lithography, Ar^+ ion milling, and reactive ion etching were used to fabricate three-terminal lateral devices with a backside gate electrode, illustrated in Fig. 1(a) [9]. As shown in Fig. 1(b), the source-drain current I_{21} value gradually increases for all the source-drain voltage (V_{SD}) with increasing gate voltage (V_G). This means that the conduction channel is formed from the vicinity of the interface between SOI and BOX. These results clearly indicate that this device can operate as a MOSFET.

3. Detection of spin accumulation in Si

The three-terminal Hanle-effect measurements were performed at room temperature by a dc method with the current-voltage configuration shown in Fig. 1(a), where a small magnetic field perpendicular to the plane, B_Z, was applied after the magnetic moment of the contact 2 aligned parallel to the plane along the long axis of the contact. Figure 2(a) shows the room-temperature voltage change (ΔV_{23}) as a function of B_Z (ΔV_{23}–B_Z curve) for V_G = 8.0 V at I_{21} = -1.0 μA, where a quadratic background voltage depending on B_Z is subtracted from the raw data. In this condition (I_{21} < 0), the electrons are injected from the spin-polarized states of CoFe into the conduction band of Si. When B_Z increases from zero to ± 200 Oe, a clear voltage

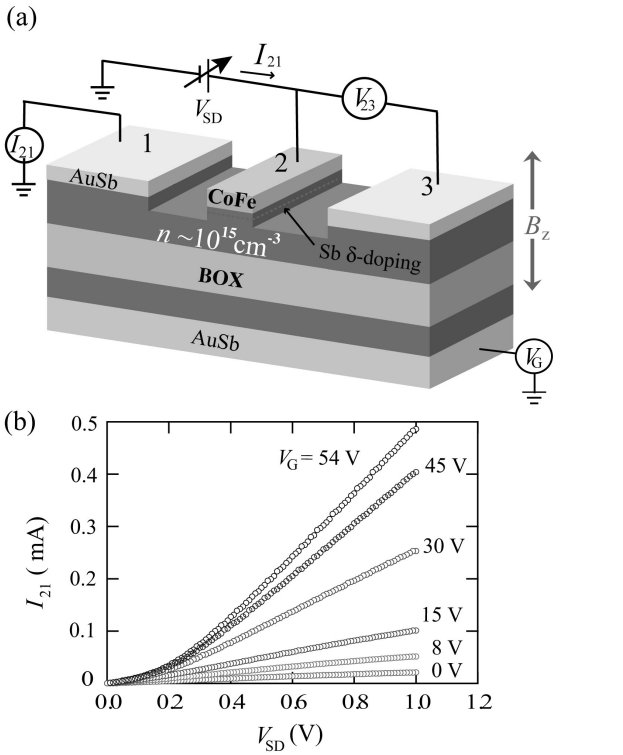

Fig.1. (a) Diagram of a Si-MOSFET with a CoFe/n$^+$-Si Schottky-tunnel-barrier contact. (b) I_{21} - V_{SD} curves for various V_G values at room temperature.

change ($|\Delta V_{23}|$) is observed even at room temperature.

The magnitude of ΔV_{23} ($|\Delta V_{23}|$) is ~11.5 μV. When the gate voltage is further applied up to V_G = 54 V [Fig. 2(b)], $|\Delta V_{23}|$ is decreased to ~7.8 μV surprisingly despite the same value of the injection current (I_{21} = -1.0 μA). For both V_G conditions, a lower limit of spin lifetime (τ_S) can be obtained using the Lorentzian function,[4] $\Delta V_{23}(B_Z) = \Delta V_{23}(0)/[1+(\omega_L\tau_S)^2]$, where $\omega_L = g\mu_B B_Z/h$ is the Lamor frequency, g is the electron g-factor (g = 2), μ_B is the Bohr magneton. The fitting results are denoted by the solid curves in Figs. 2(a) and (b). The τ_S values for V_G = 8.0 and 54 V are estimated to be ~ 1.30 and ~ 1.27 nsec, respectively.

According to the simple spin-diffusion model,[10] we can analyze the magnitude of the observed spin signals. The voltage change (ΔV) can be expressed as $P\lambda_N\rho_N I_{21} / 2A$, where P is the spin polarization, λ_N and ρ_N are the spin diffusion length and resistivity of the nonmagnet used, respectively. A is the contact area (100 μm^2). For our fabricated device, λ_{Si} ~ 2.3 μm is obtained [9]. Also, ρ_N =1–5 Ωcm at room temperature is assumed. Since the spin resistance-area-product (spin-RA), $(\Delta V_{23}/ I_{21})A$, is obtained to be ~ 1.15 kΩμm^2 for the data in Fig. 2(a), we can roughly obtain $0.14 < P < 0.32$. This value is consistent with that for CoFe alloys reported [11]. Therefore, our data observed here can roughly be considered within the framework of the commonly used diffusion model [10].

Furthermore, the reduction in the $|\Delta V_{23}|$ can be explained. Schematic diagrams of the spin accumulation in the Si channel beneath the CoFe/n^+-Si contact are shown in Fig. 2(c). Under a condition for spin injection into Si, the spin accumulation ($\Delta\mu$) occurs in the Si conduction band near the quasi Fermi level (left figure). When we increase V_G from V_{G1} to V_{G2}, the carrier density in the Si conduction channel beneath the CoFe/n^+-Si contact increases, causing the decrease in channel resistance. Namely, even if the same I_{21} is used for spin injection into the Si channel, tunneling probability of spin-polarized electrons and the density of state in Si at the Fermi level should be varied by the application of V_G, resulting in the reduction in $\Delta\mu$ (right figure). Therefore, this feature indicates reliable evidence for the spin injection into an intrinsic Si channel. This study includes a technological jump for Si-based spin MOSFET.

4. Summary

We have demonstrated electric-field control of spin accumulation in Si using a MOSFET structure with a CoFe/n^+-Si contact. Even at room temperature, we observed clear spin accumulation signals under an application of the gate voltage. The magnitude of the spin accumulation signals was reduced by the increase in the gate voltage. We consider that the reduction in the spin-accumulation signals is attributed to the increase in the carrier density in the Si channel beneath the CoFe/n^+-Si contact, indicating reliable evidence for the spin injection into the semiconducting Si channel at room temperature. This study also includes a technological jump for Si-based spin MOSFET.

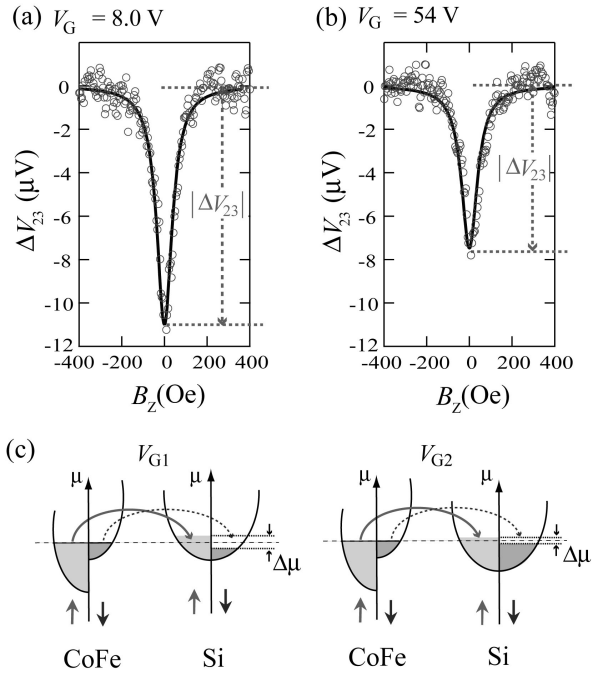

Fig. 2. (a) Room-temperature spin accumulation signals measured at V_G = (a) 8.0 V and (b) 54 V. The applied bias current is a constant value of I_{21} = -1.0 μA, which induces spin accumulation in a Si conduction band by spin injection from CoFe into Si. The solid curves are fitting results by the Lorentzian function. (c) Schematic diagrams of the change in the spin accumulation by the application of V_G.

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