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Effects of Trap Energy Levels on Reverse Recovery Surge of Silicon Power Diode

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1. Introduction

The reverse recovery surge of silicon diodes has been intensively investigated with a view to suppress the surge voltage and EMI noise. In order to realize a soft recovery, an optimization of excess carrier distribution in the diode has been performed by carrier lifetime control [1]. In a recent study [2], the carrier lifetime profile was optimized and the current dependency of the surge voltage was improved by backside laser annealing. However, the reverse recovery characteristics have an influence on not only the carrier lifetime profile but also the trap energy levels. The relationship between the trap energy levels and the surge voltage has not yet been made clear.

This is the first paper reporting on the effects of trap energy levels on the surge voltage. The current and temperature dependency of the surge voltage with different trap energy levels was investigated. We found that in efforts to achieve soft recovery in the design of the silicon power diodes, the trap energy levels play a crucial role along with the carrier lifetime profile.

2. Silicon Power Diode

In order to investigate the relationship between the trap energy levels and the surge voltage, He-irradiated and the Pt-diffused diodes were prepared. DLTS measurements as shown in Figure 1 revealed that the main peaks of the diodes in which Pt and He were introduced corresponded to E_t-E_i=0.32eV and 0.1eV, respectively.

3. Results and Discussion

Figure 2 shows the measured current and temperature dependency of the surge voltage with different lifetime control methods. The maximum surge voltage was generated when the current was low in the case of the He-irradiated diode, and when the current was high in the case of the Pt-diffused diode. In addition, the surge voltage of the Pt-diffused diode decreased with increase in temperature. Figure 3 shows the simulated current and temperature dependency of the surge voltage with shallow (E_S) and deep (E_D) level traps. Uniform distribution of the trap density in the depth direction was assumed. The simulated results are similar to the measurements. This indicates that the current and temperature dependency of the surge voltage can be affected by the trap energy levels.

There is a strong correlation between surge voltage and excess carrier distribution just before the diode turn-off. The excess carrier distribution (p_n) in the depth direction (x) is expressed as [3],

$$p_n(x) = A\left\{\frac{\cosh(x/L)}{\sinh(W/2L)} - B\frac{\sinh(x/L)}{\cosh(W/2L)}\right\} \qquad (1)$$

where W and L are the drift width and ambipolar diffusion length, respectively, and A and B are coefficients for the functions of p_n and recombination rate (R_r), respectively [3]. Then, the relationship between p_n and R_r with various trap energy levels can be established using the SRH model as follows [4],

$$R_r = \frac{\sigma v_{th} N_T p_n^2}{2\left[p_n + n_i \cosh\{(E_t - E_i)/kT\}\right]} + \frac{p_n}{\tau_{bulk}} \qquad (2)$$

where σ is the capture cross section, v_{th} is the thermal velocity, N_T is the trap density, τ_{bulk} is the intrinsic carrier lifetime in the drift region. Figure 4 shows the correlation between R_r and p_n calculated with Eq. (2). Note that the R_r with the E_S (R_{rS}) and E_D (R_{rD}) exhibit a different p_n and temperature dependence, that is, $R_{rD}>R_{rS}$ with low p_n and $R_{rD}<R_{rS}$ with high p_n. Moreover, R_{rS} depends strongly on the temperature.

Figure 5 shows a comparison of the calculated carrier distribution in the depth direction of the two trap energy levels obtained with Eqs. (1) and (2). The carrier density is normalized at the junction X=0. Here, the carrier density with E_S is p_{nS}, and E_D is p_{nD}. At the junction X=W, $p_{nD}<p_{nS}$ with low current and $p_{nD}>p_{nS}$ with high current. This is due to variations in the injected carrier density resulting from differences in the recombination rate, as seen in Figure 4. The surge voltage becomes higher with decrease in p_n adjacent to the cathode relative to that of the anode (dashed circles depicted in Figure 5). Therefore, the surge voltage with E_S is essentially lower with low current, and higher with high current than the E_D. In the case of elevated temperature, p_{nS} increases and the surge voltage decreases with increase in temperature as shown in Figure 6.

From this numerical analysis based on the SRH model, it was confirmed that variations in recombination rate due to trap energy levels have an influence on the current and temperature dependency of surge voltage.

4. Conclusions

In summary, the effects of trap energy levels on the surge voltage in the Silicon power diodes were demonstrated. It became clear that variations in recombination rate due to trap energy levels have an influence on the surge voltage. The trap energy levels in the silicon power diode play an important role in design for soft switching as well as the carrier lifetime profile.

References

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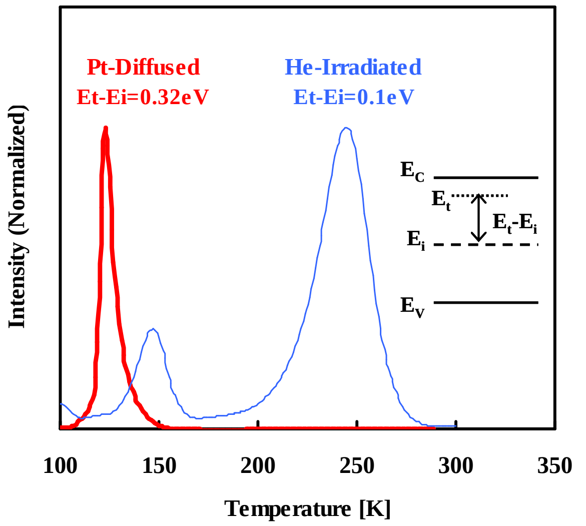

Fig. 1 Measured DLTS spectra with each lifetime control method.

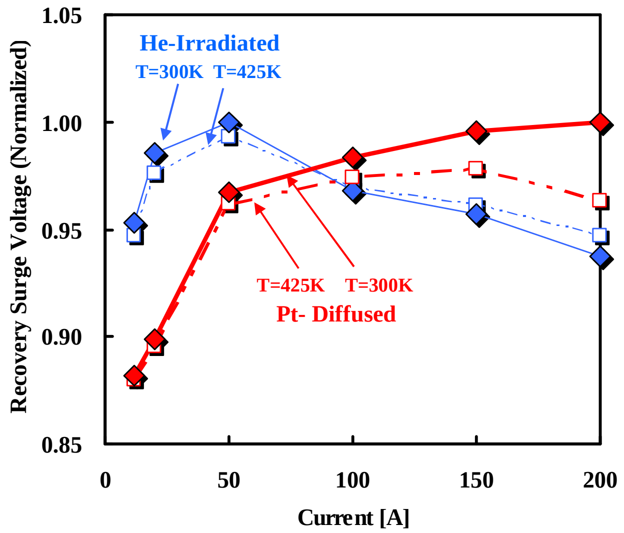

Fig. 2 Measured current and temperature dependency of recovery surge with each lifetime control method.

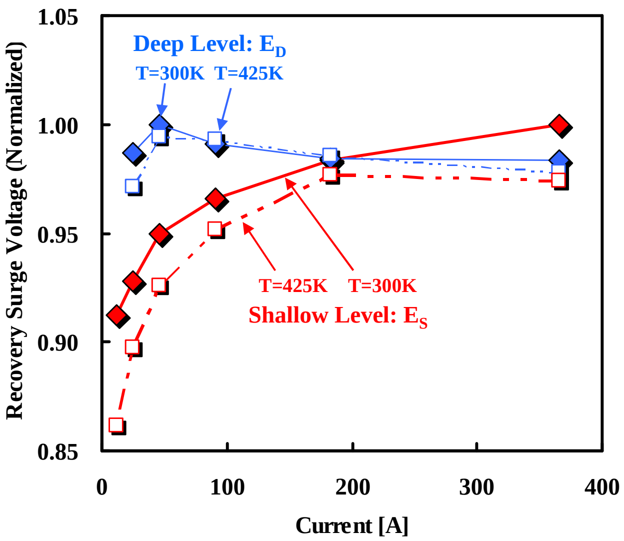

Fig. 3 Simulated current and temperature dependency of recovery surge with each trap energy level.

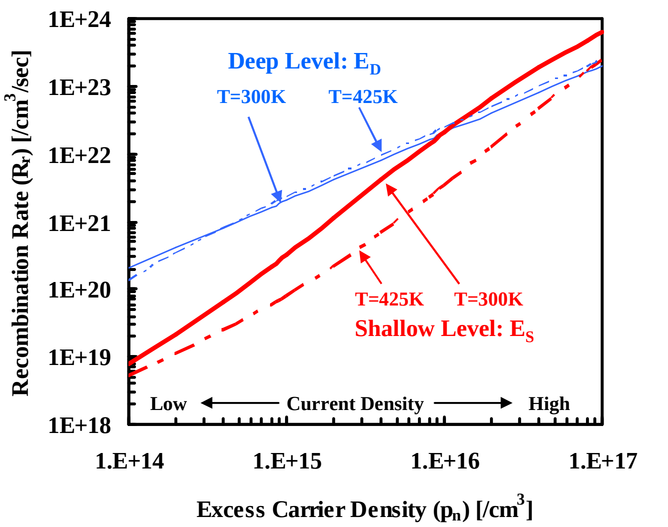

Fig. 4 Calculated correlation between recombination rate and excess carrier density.

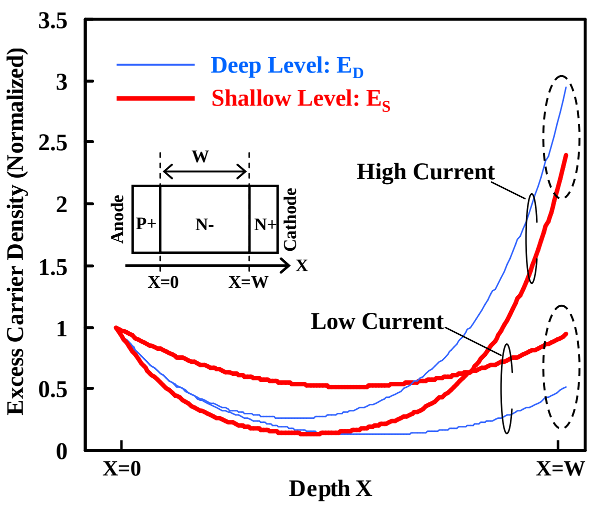

Fig. 5 Comparison of excess carrier distributions with different current and trap energy levels.

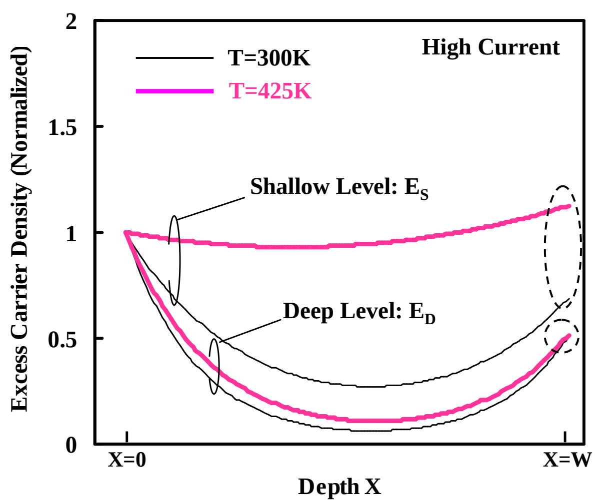

Fig. 6 Comparison of excess carrier distributions with different temperature and trap energy levels.