Compact Modeling of Floating-Base Effect in IGBT Based on Potential Modification by Accumulated Charge

Takao Yamamoto¹, Masataka Miyake² and Mitiko Miura-Mattausch²

¹ DENSO CORPORARATION, 1-1 Showa-cho, Kariya-shi, Aichi 448-8661, Japan Phone: +81-566-63-1925 E-mail: takao_o_yamamoto@denso.co.jp ² Advanced Sciences of Matter, Hiroshima University 1-3-1 Kagamiyama Higashi-Hiroshima, Hiroshima 739-8530, Japan

Abstract

We have developed a compact model of the Injection-Enhanced Insulated-Gate-Bipolar Transistor applicable for circuit optimization. The main development is modeling the hole accumulation in the floating-base region. It is demonstrated that observed negative gate capacitance is well reproduced with the developed model.

1. Introduction

The IGBT (Insulated-Gate-Bipolar Transistor) structure realizes the high current controllability together with the high breakdown voltage. Because of these advantages, the IGBT structure has been widely applied for inverter circuits of power electronics. Therefore many descendants of IGBT have been developed according to the different applications purposes. The IEGT (Injection-Enhanced Insulated-Gate-Bipolar Transistor) structure has been developed in order to reduce the on-state voltage [1], which results in the soft switching waveform in comparison to that of IGBT. Thus, IEGT has been applied to the area where reduced voltage overshoot is required. However, the soft waveform causes large switching loss at the same time. To optimize the trade-off between the low overshoot and the low energy-loss, accurate circuit simulation for investigating the switching performance is inevitable.

HiSIM-IGBT has been developed for simulating circuit performances, which solves the potential distribution within IGBT explicitly [2]. However, it considers the symmetrical IGBT structure. The purpose of this investigation is to extend HiSIM-IGBT for the asymmetrical IEGT structure (see Fig. 1). For the purpose we consider the accumulated charge induced in the floating- base region explicitly.



Fig. 1. Comparison of two IGBT structures, (a) the symmetrical IGBT structure, and (b) the asymmetrical IEGT structure.

2. Switching Response of Floating-Base

Fig. 2a shows the studied basic circuit with its element values. Measurements and results with HiSIM-IGBT for the asymmetrical structure are compared in Fig. 2b. The difference between the two waveforms denoted by a dashed circle is attributed to the floating-base effect.

The floating-base effect is investigated with 2D-device simulations [3]. Fig. 3 shows simulated gate capacitance C_{gg} divided into different contributions. Fig. 4 shows equi-hole-density contours around the gate oxide. The contacted p-base side forms the inversion layer, when V_{ge} reaches the threshold voltage (V_{ge} =7.4V). On the other hand, the floating-base side does not form the inversion layer at V_{ge} =7.4V. Beyond the threshold condition the collector current flows into the floating-base as well, and increases the potential drastically. This hole accumulation causes "negative capacitance [4, 5]".



Fig. 2. (a) Studied basic circuit and their element values, (b) Measured transient characteristics in comparison to those of simulation results with original HiSIM-IGBT.



Fig.3 2D-device simulation result of gate capacitance for floating -base structure at V_{ce} =600V, freq=0.001Hz, V_{ge} sweep. (b) Zoomed result denoted by a dashed rectangle depicted in (a).



Fig.4 Simulated hole-density distributions around the gate. $[/cm^3](V_{ce}=600V)$

The negative capacitance reduces abruptly at V_{ge} =7.5V as shown Fig. 5a. This abrupt decrease of C_{gg} coincides with the saturation behavior of the floating-base potential $V_{\rm fp}$. The hole accumulation charge changes the potential $V_{\rm fp}$. Fig. 5b shows the width (W_{float} : see Fig. 1b) dependence of $C_{\rm gg}$. Though the increase of $W_{\rm float}$ shows no influence, the decrease causes the delay of the switching from the accumulation to the depletion condition, because the total amount of the injected holes in the floating-base region is reduced with reduced W_{float} . Further increase of V_{ge} induces the inversion condition, which causes the positive C_{gg} as shown in Fig. 6.



Fig. 5. (a) 2D-device simulation results of C_{gg} , floating-base voltage and I_c current for floating-base structure. (b) 2D-device simulation result of the width (W_{float}) dependence of C_{gg}



3. Modeling of Floating-Base Effect

Modeling of the floating-base effect is done by considering the n-MOS capacitance as shown Fig.7, where $V_{\rm fp}$ is the node potential introduced to describe the floating-base effect induced by hole injection. The hole injection into the floating-base occurs because the base potential is higher than $V_{\rm fp}$ and continues until $V_{\rm fp}$ becomes larger than the internal base potential. In HiSIM-IGBT the base node is calculated by solving the Kirchhoff equation explicitly. Since all node potentials are precisely determined, the carrier movement within the device can be predicted in a consistent way. Once V_{ge} reaches the threshold condition and the collector current starts to flow, a large amount of the hole injection into the floating-base occurs and increase the $V_{\rm fp}$ potential drastically, resulting in the transition into the accumulation condition.

The developed equivalent circuit shown in Fig. 7 is written in the Verilog-A code and tested with a commercial SPICE simulator. A calculation result of the negative C_{gg} due to the hole injection is shown in Fig. 8 in comparison to the 2D-device simulation results. The model reproduces the 2D-device simulation result quite well. For better fitting, the resistance effect between the base potential and $V_{\rm fp}$ could be considered. The neglected built-in potential between the floating-base and the n-base could also play a role.



Fig. 7. Equivalent circuit of the developed model.



Fig. 8. Calculated gate capacitance with the developed model as a function of V_{ge} in comparison to 2D-device simulation result. (b) Zoomed result denoted by a dashed rectangle depicted in (a).

4. Conclusions

We have developed the negative gate capacitance model observed in the IEGT structure based on the hole injection into the floating-base. The model has been implemented into a circuit simulator and verified the accuracy.

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