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Point Defect Reduction and Carrier Lifetime Improvement of Si- and C-face 4H-SiC Epilayers

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1. Introduction

Silicon carbide (SiC) is one of the promising wide band gap semiconductor materials which can realize very high-voltage (>10 kV) electronic devices. For high-voltage applications, bipolar devices are desirable due to the low forward voltage drop originating from the conductivity modulation in thick and low-doped drift layers. In n-type 4H-SiC epilayers, the $Z_{1/2}$ center is recognized as a major lifetime killer that is an intrinsic point defect likely related to a carbon vacancy. The $Z_{1/2}$ center frequently limits the carrier lifetime in epilayers, and degrades the electrical characteristics under forward biased mode operation of bipolar devices. Post-growth processes including the carbon ion (C^+) implantation/annealing process [1] and the thermal oxidation/annealing process [2], were proposed to reduce the $Z_{1/2}$ center concentration in the epilayers.

In this study the optimum conditions of the C^+-implantation/annealing process for thick (>100 μm) epilayers are investigated. The effects of C^+-implantation/annealing process and thermal oxidation/annealing process are investigated for both Si- and C-face epilayers.

2. Experimental

Sample Preparation

Thick epitaxial layers were grown on 4H-SiC (0001)Si-face or (000-1)C-face of 8° off-axis commercial substrates in a vertical hot wall reactor. The thickness and the nitrogen doping concentration of the Si-face epilayer are ~140 μm and 2-3×10^{14} cm^{-3}. The thickness and the nitrogen doping concentration of the C-face epilayer are ~100 μm and 5×10^{14} cm^{-3}, respectively.

Two post-growth processes were applied to the epilayers. In the C^+ implantation/annealing process, carbon ions were implanted into the epilayer surface to form 250 nm box-profile with the concentration of 5×10^{18} cm^{-3} or 5×10^{20} cm^{-3}, and subsequent annealing was performed for 30 min at the range from 1300 to 1800 °C. In the thermal oxidation/annealing process, the oxidation temperature was 1200-1300 °C and the time was 5 h once or twice. The oxide layer was removed before the annealing at 1550 °C for 30 min.

Evaluation of Carrier Lifetime and Point Defect

Carrier lifetimes of the epilayers before and after the post-growth processes were measured by time-resolved photoluminescence (TRPL) at room temperature. Concentrations of the $Z_{1/2}$ center were measured with deep level transient spectroscopy (DLTS). Successive polishing and DLTS measurement were conducted to obtain depth-profiles of the $Z_{1/2}$ center concentration.

3. Results and Discussion

The carrier lifetimes of Si-face epilayers before and after the post-growth processes were shown in Fig. 1. The carrier lifetime of the as-grown sample was ~2 μs. After C^+ implantation/annealing process, the carrier lifetimes increased with the annealing temperature, and surpassed 10 μs by 1600 °C annealing. However, the carrier lifetimes turned to decrease at temperatures higher than 1700 °C. We have confirmed an increase of the $Z_{1/2}$ center concentration at the deep region of the epilayer after 1800 °C annealing. This agrees with a literature, which reported that the $Z_{1/2}$ center concentration increases and the carrier lifetime decreases after high-temperature annealing at above 1700°C [3]. In consequence the annealing temperature of 1600 °C can be optimum for the lifetime enhancement. The Carrier lifetimes were not significantly affected by the C^+ implantation concentration within the experimental conditions studied.

After thermal oxidation/annealing process, the carrier lifetime was enhanced as well. As the oxidation temperature and/or time increased, the carrier lifetime increased. After oxidation at 1300 °C for 5h twice and annealing, the carrier lifetime surpassed 10 μs.

Figure 2 shows the depth profiles of the $Z_{1/2}$ center concentration of Si- and C-face epilayers after post-growth processes. The process conditions were chosen to obtain the longest carrier lifetimes shown in Fig. 1. The $Z_{1/2}$ center concentrations of as-grown epilayers were 1-3×10^{12} cm^{-3} for Si-face, and 2×10^{13} cm^{-3} for C-face. The C^+ implantation/annealing process eliminated the $Z_{1/2}$ center to the depth of 100 μm for Si-face and 50 μm for C-face. The relatively high initial $Z_{1/2}$ center concentration in the C-face epilayer resulted in the shallower depth of $Z_{1/2}$ center free region. The thermal oxidation/annealing process also eliminated the $Z_{1/2}$ center to the depth of 100 μm for the Si-face epilayer. However, for the C-face epilayer, the $Z_{1/2}$ center concentration was reduced near the surface only, and became comparable to that of the as-grown material at deeper region.

The $Z_{1/2}$ center elimination process can be divided into 2 steps; emission of carbon atoms from the implanted layer or the oxide/SiC interface, and diffusion into deeper region.

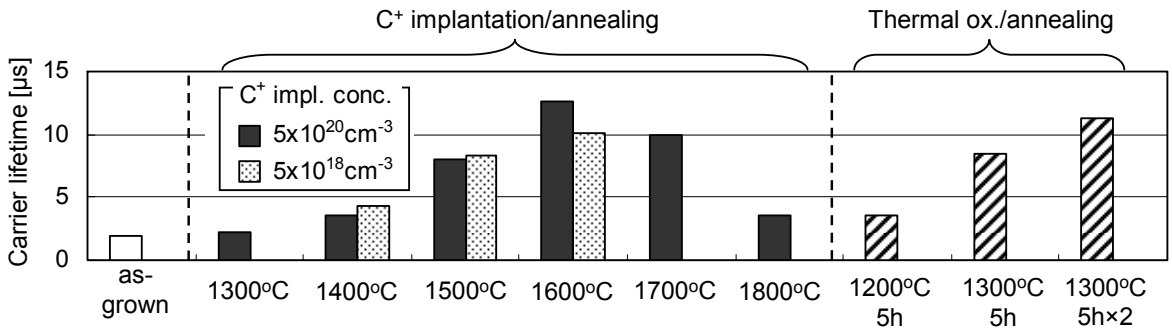

Fig. 1 Carrier lifetimes of 4H-SiC epilayers on Si-face before and after post-growth processes.

It is not likely that the diffusion coefficients of carbon interstitials in SiC crystals differ significantly for [0001] and [000-1] directions. Actually the $Z_{1/2}$ center concentration in the C-face epilayer was significantly reduced by the C^+ implantation/annealing process. Therefore, the carbon emission phenomenon at the oxide/SiC interface may be different for Si- and C-face, and the carbon emission rate to SiC crystal should be smaller for oxidation on C-face. This is one of the possible reasons for the slight $Z_{1/2}$ center reducing effect of thermal oxidation/annealing process on C-face.

Figure 3 shows the TRPL decay curves of the C-face epilayer before and after the post-growth processes. The carrier lifetime of as-grown sample was 0.13 μs due to the relatively high initial concentration of $Z_{1/2}$ center compared to Si-face epilayers. After the thermal oxidation/annealing process, no significant change was observed in the decay curve. On the other hand, the carrier lifetime of the epilayer after the C^+ implantation/annealing process was obviously enhanced to 0.66 μs. The results of the carrier lifetime measurement agree with the depth profiles of $Z_{1/2}$ center concentrations in C-face epilayers.

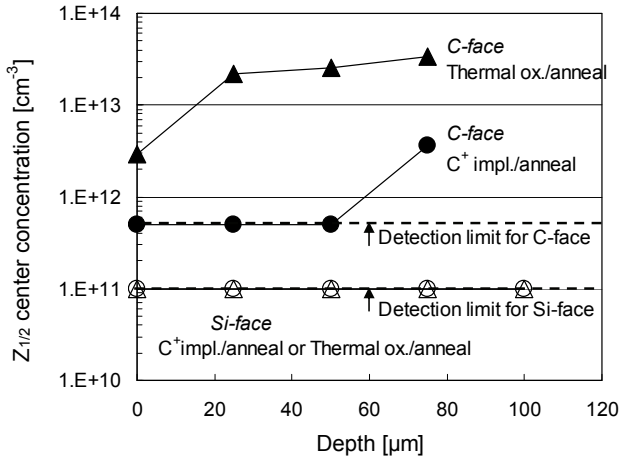

Fig. 2 Depth profiles of $Z_{1/2}$ center concentration in Si- and C-face epilayers after post-growth processes. The C^+ implantation concentration and the annealing temperature were 5×10^{20} cm^{-3} and 1600 °C. The oxidation temperature and time were 1300 °C and 5h twice.

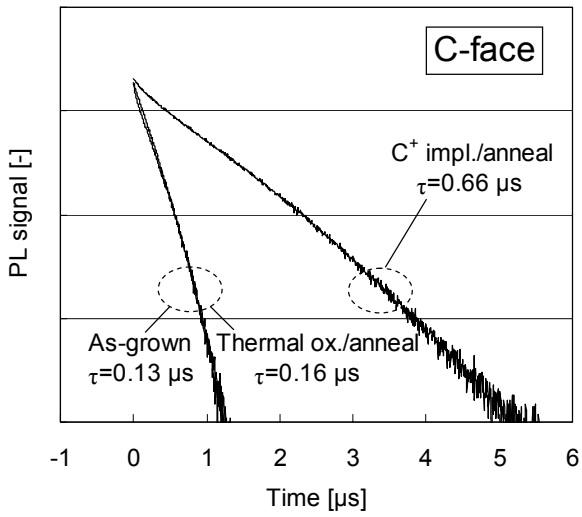

Fig. 3 TRPL decay curves of C-face epilayers before and after post-growth processes. The C^+ implantation concentration and the annealing temperature were 5×10^{20} cm^{-3} and 1600 °C. The oxidation temperature and time were 1300 °C and 5h twice.

4. Conclusions

By applying the post-growth processes, the $Z_{1/2}$ center concentration is reduced and the carrier lifetime in Si-face epilayers is significantly enhanced to over 10 μs (epilayer thickness of ~140 μm). The C^+ implantation/annealing process is also effective for the $Z_{1/2}$ center reduction and carrier lifetime improvement of C-face epilayers.

Acknowledgements

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References

[1] L. Storasta and H. Tsuchida, Appl. Phys. Lett. **90** (2007) 062116.

[2] T. Hiyoshi and T. Kimoto, Appl. Phys. Express **2** (2009) 091101.

[3] B. Zippelius, J. Suda and T. Kimoto, J. Appl. Phys. **111** (2012) 033515.