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Suppression of Al Memory Effect on Growing 4H-SiC Epilayers by Hot-wall Chemical Vapor Deposition

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1. Introduction

Silicon carbide (SiC) materials, especially the poly-type of 4H-SiC is very competitive to traditional Si in certain application fields like high power, high frequency devices. Recently, attentions are attracted on the promotion of productivity and the development of novel devices. The chemical vapor deposition (CVD) is the most popular method due to the benefit capable of growing 4H-SiC epilayers with uniform thickness and doping concentration throughout a large area. However, in p-type 4H-SiC CVD growth, it is found that memory effect is rather strong: the formerly deposited SiC (on wafer, susceptor or reactor wall) releases p-dopants acting as an additional doping source [1]. The severe case observed from the junction field effect transistor (JFET) adopting a heavily Al-doped (N_{Al}~10^{19} cm^{-3}) layer under an undoped or lightly n-doped layer, is the unpredictable changing of conductivity type of n-doped layer [1]. Similar problem may delay the practical application of the insulated gate bipolar transistor (IGBT) that requires p^+ layer underneath n-doped layers because of lacking low resistivity p^+ 4H-SiC substrates [2]. The resistivity of above p^+ layer is expected around ~10 mΩ·cm [3], corresponding to a net acceptor density (N_A-N_D) higher than 10^{19} cm^{-3}. Obviously, the grown p^+ layers for both JFET and IGBT are not ready for transferring into n-reactor in view of possible contaminations. Therefore, in-situ (in same reactor) formation of low Al cover layer by suppressing Al memory effect to an acceptable level as well an abrupt Al distribution is more sensible to device fabrication.

About Al memory effect, seldom works have been reported [1,3-5]. One conclusive solution has been made as growth in separate reactors for n/p layers [4]. It is inapplicable in considering of contaminations. Besides, device by a continual growth demonstrates superior performance than that by an interrupted growth [6]. As for in-situ suppression of Al memory effect, Schöner *et.al* suggested a high temperature "cleaning" by baking stored Al out [1], but it requires wafer out-loading. La Via *et.al* reported the growth with trichlorosilane. It may cause a doping limit of 1×10^{18} cm^{-3} [7]. Nordell *et.al* investigated the Al doping behavior by adding HCl and at the same time varying C/Si ratios [5]. Abrupt Al distributions between doped and undoped layers (N_{Al} at surface layers 10^{19} to 2×10^{15} cm^{-3}; inner layers 1.5×10^{20} to 7×10^{15} cm^{-3}) have been obtained. However, HCl etching process might degrade the series resistance was detected, when evaluating p-i-n diodes.

This work investigates the relevant Al memory effect in 4H-SiC CVD growth, in view of device structure including a heavily Al-doped layer, and intends to suppress Al impurities to an acceptable level by varying C/Si ratio and temperature within one continual growth run.

2. Experimental and Results

Experimental

A commercial type horizontal hot-wall chemical vapor deposition system equipped with standard precursors, silane (SiH_4), propane (C_3H_8) and trimethylaluminium (TMA) was employed. On as-received 3" n-type 8° off-oriented 4H-SiC wafer, the growth was carried out at the pressure of 10 kPa. The TMA flow rate was set in 40 sccm. SiH_4 was supplied in 30 or 60 sccm, while C_3H_8 flow rate was varied in the range of 4~20 sccm in C:Si mole ratios of 0.4~1. The whole system is computer controlled that ensures a quick and precise switching of gaseous precursors' turn-on/-off operations. Secondary ion mass spectrometry (SIMS) was used to obtain Al dopants and impurities concentration in multilayer samples. Capacitance-Voltage (CV) measurement was used to estimate doping level in single 4H-SiC epilayer. The epilayer thickness was measured by Fourier transform infrared spectroscopy (FT-IR).

Results

Figure 1 shows SIMS profile of a multilayer structure of Al-doped layers and undoped interlayers. After Al heavy doping, N_{Al} decreases to 2×10^{18} cm^{-3}, nearly two orders (~1/50) lowered. After 1st Al-doped layer (P1) growth, TMA flow was switched off, while SiH_4 and C_3H_8 were kept open to precede undoped interlayer growth. Its profile is rounder than the interlayer after 2nd Al-doped layer (P2) growth, where 1 minute interval of source gases (only H_2 flow) was introduced. The round corners on top of doping spike relating to strong adsorption/desorption of Al species on reactor wall [5] cannot be seen, which implies that the main source of Al impurities in interlayer is decomposition (H_2 etching) of formerly deposited Al:SiC alloy in reactor,

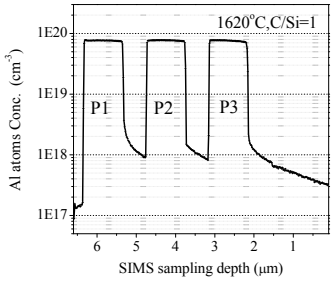

Fig. 1 SIMS profile of multilayers with heavily Al-doped and undoped layers grown at 1620 °C and C/Si=1.

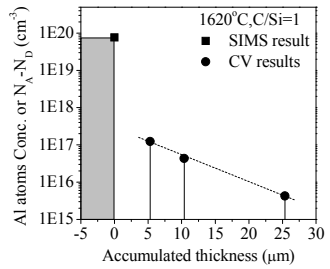

Fig. 2 SiC coverage effect: A 5 μm thick heavily Al-doped growth run and three following undoped growth runs at C/Si=1.

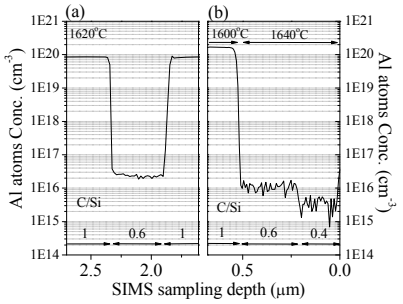

Fig. 3 SIMS profiles of two samples with Al-doped layers and undoped layers grown at various C/Si ratios and temperature of (a) 1620 °C , (b) 1600 and 1640 °C .

and it cannot be diminished by short H_2 purging due to concurrent H_2 etching.

In order to examine Al impurities background level in using SiC coverage, a series of undoped 4H-SiC layers were grown after a 5 μm thick heavily Al-doped layer. In Fig. 2, CV results reveal a linearly decreasing of doping level N_A-N_D (a proportion of N_{Al}) in logarithm scale and the doping level was reduced to 10^{15} cm^{-3} level by the deposition of 25 μm in thickness. A thick coverage layer makes it impossible to build an abrupt Al distribution between two adjacent layers which is indispensable for device formation.

Based on above results, we have tried to minimize Al impurities level by hindering Al atoms incorporation using site competition growth (Si-rich) [8] and by enhancing desorption of Al atoms at higher temperature. Figure 3(a) presents SIMS profile of a structure with heavily Al-doped layers and an undoped interlayer at varied C/Si ratios. By changing C_3H_8 flow to 6 sccm (C/Si=0.6), a relatively abrupt Al distribution is obtained. The undoped interlayer exhibits a uniform N_{Al}~2.5×10^{16} cm^{-3}. Comparison of the undoped interlayers in Fig.1 and Fig. 3(a) knows that the excessive Si species (C/Si=0.6) efficiently hinder Al incorporation, and thus bring an additional two orders reduction of Al impurities level.

Figure 3(b) gives the results of enhancing desorption of Al atoms. A heavily Al-doped layer (N_{Al}=1.7×10^{20} cm^{-3}) was formed by lowering temperature to 1600 °C at the same time setting C/Si=1 (SiH_4=60, C_3H_8=20 sccm). Elevating temperature to 1640 °C and decreasing C/Si to 0.6 (SiH_4=30, C_3H_8=6 sccm) made N_{Al}=1×10^{16} cm^{-3} even if it started from a higher N_{Al} against that in Fig. 3(a). Further changing C/Si ratio to 0.4 reduced N_{Al} to 3×10^{15} cm^{-3}. Consequently, a rather abrupt Al distribution in a magnitude of 17,000 (possible to 50,000), between Al-doped and undoped layers grown at varied temperatures, was achieved. It is verified that making a combination of temperature elevation and site competition effects can remarkably suppress the Al memory effect in 4H-SiC CVD growth.

3. Conclusions

The Al memory effect in growing 4H-SiC by traditional hot-wall CVD was investigated. By varying C/Si ratio, the employed site competition growth successfully suppresses Al memory effect and creates a uniform Al impurities level. Growth temperature is confirmed workable to hinder Al incorporation into SiC lattice, at an elevated temperature. A heavily Al-doped layer of 1.7×10^{20} cm^{-3} with a convincing low resistivity was attained, covered by an undoped layer down to N_{Al} ~3×10^{15} cm^{-3} that is adequate low to n-doping even in a single reactor. The achieved results are valuable to devices fabrication involving a heavily Al-doped layer. Detailed characterizations and the growth at various C/Si ratios and temperature will be reported on the conference.

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