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Transistor Characteristics of Lateral MOSFETs with a Thin 3C-SiC Layer on an Insulator

Hidetsugu Uchida, Akiyuki Minami, Toyokazu Sakata,
Hiroyuki Nagasawa and Motoki Kobayashi

HOYA Corporation
1-17-16 Tanashioda, Chuo, Sagamihara, Kanagawa, 252-0245, Japan
Phone: +81-42-777-5404 E-mail: Hidetsugu_Uchida@sngw.rdc.hoya.co.jp

1. Introduction

Since 3C-SiC MOSFETs were published in the late 1980's [1], those have been reported to show excellent transistor performances and high channel mobility [2-3]. A remaining large technical issue of the 3C-SiC devices is large leakage currents at PN junctions due to stacking faults [4]. Since MOSFETs involve PN junctions, the leakage currents should be reduced. One of the reduction methods is to reduce an electric field applied at the PN junction because the leakage current increases exponentially with the electric field. In order to reduce the electric field, we employed a thin 3C-SiC layer on an insulator for fabricating the lateral MOSFETs. In this paper, the transistor performances and blocking characteristics of the PN junctions are experimentally investigated.

2. Device Fabrication

Fig. 1 shows a schematic cross-section of a lateral 3C-SiC power MOSFET fabricated in this work. The lateral MOSFETs and PN diodes were fabricated on 3C-SiC (001) substrates with 13 µm-thick epilayers with a nitrogen concentration of $1x10^{16}$ cm^{-3} by the following process steps: (1) room temperature implantations of Al and P masked by photoresists, (2) activation annealing at 1600 °C, (3) thermal growth of gate oxides at 1150 °C in H_2O containing oxygen gas, (4) deposition of polysilicon-metal gates covered with TiW, and (5) Al interconnection with Ti and TiN layers as a diffusion barrier.

After the device fabrication, the processed wafer was lapped to less than 10 µm of the total thickness including Al interconnections and then polished with chemical mechanical polishing (CMP). The thinned wafer was attached on a Si wafer with an insulating tape.

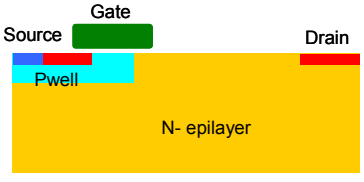

Fig.1 Schematic cross-section of a lateral 3C-SiC power MOSFET.

3. Results and Discussion

Typical output characteristic of a lateral 3C-SiC power MOSFET is indicated in Fig.2. The lateral MOSFET shows good transistor performance. As shown in Fig.3, the leakage current at the negative gate voltages is very low in the transfer characteristic.

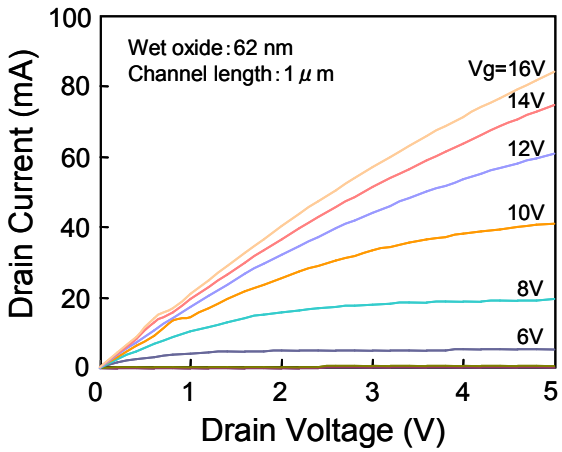

Fig.2 Output characteristic of a lateral power MOSFET.

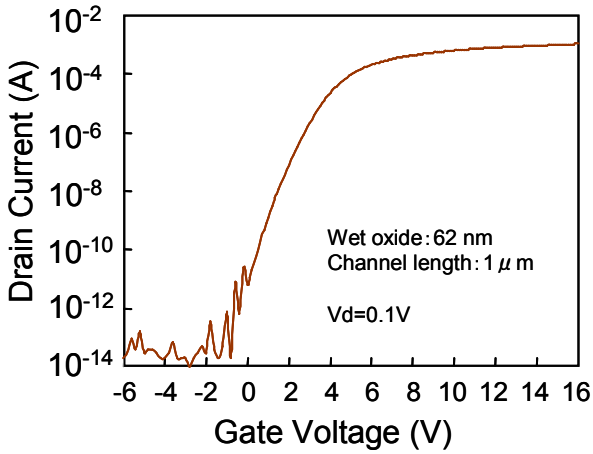

Fig.3 Transfer characteristic of a lateral power MOSFET.

A 2-dimensional device simulation suggests that the Semiconductor-On-Insulator (SOI) structure brings about the lower electric field at the PN junction with the thinner semiconductor layer. This is because the increase in an electric potential around the PN junction is strongly suppressed after the depletion layer around the PN junction extends and connects to the bottom of the semiconductor layer. In the SOI structure, lateral MOSFETs have to be adopted since the currents can not flow vertically but laterally. In order to confirm the reduction of leakage

current owing to the lowering of electric field, we thinned the processed wafer as described above.

The blocking characteristics of lateral PN diodes measured after thinning at 10 µm are shown in Fig.4. Leakage currents are found to be reduced by the thinning, especially for PN diodes with field limiting rings (FLRs). Since the FLR and SOI structure with a thin semiconductor layer can relax the electric fields mainly in the lateral and vertical directions, respectively, it is likely that the leakage currents are reduced significantly by the combination. The more reduction of leakage currents is brought by the thinner 3C-SiC layer at 6 µm as presented in Fig.5.

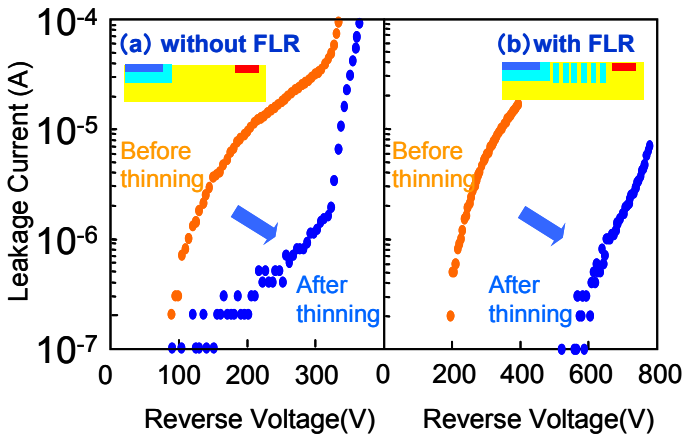

Fig.4 Blocking characteristics of 10 µm-thick lateral PN diodes (a) without and (b) with FLRs.

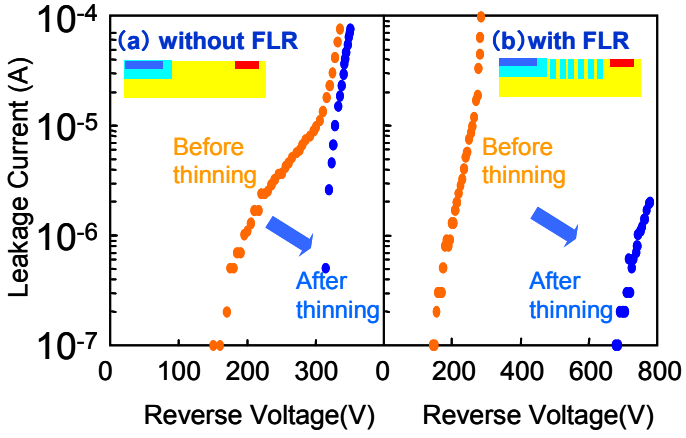

Fig.5 Blocking characteristics of 6 µm-thick lateral PN diodes (a) without and (b) with FLRs.

As shown in Fig.6, unlike the case of leakage current, a little of drain current in lateral power MOSFETs is reduced by the SiC thinning to 10 µm. Using n-channel MOSFETs without drift regions, the effect of the thinning on the channel mobility was evaluated. As a result, there is little change in the channel mobility of the n-channel MOSFETs by the thinning as illustrated in Fig.7. Based on the measurement data, the specific on-resistance of the 10 µm-thick lateral 3C-SiC MOSFETs is estimated as 13.3 mΩcm^2 in an active cell area for a voltage of 600 V.

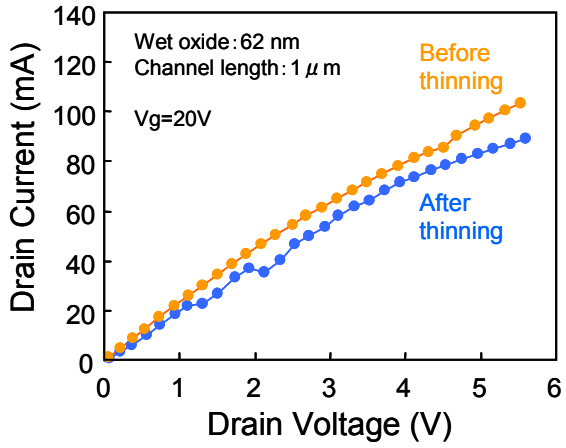

Fig.6 Drain currents of a lateral power MOSFET before and after wafer thinning.

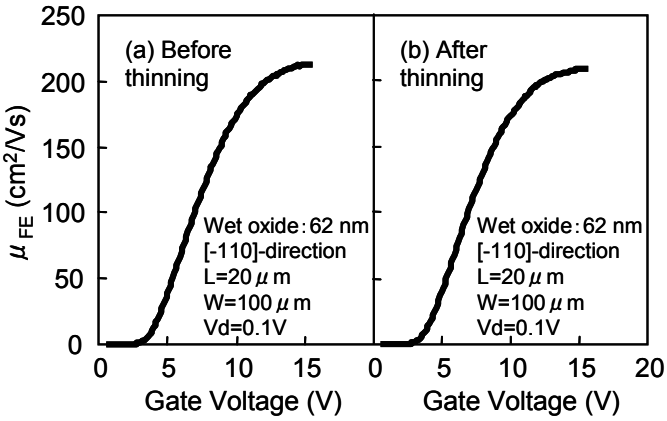

Fig.7 Channel mobility of an n-channel MOSFET (a) before and (b) after thinning.

4. Conclusions

In order to reduce the leakage currents through PN junctions, 3C-SiC wafer with device processing was thinned to less than 10 µm. The drain currents and channel mobility change little by the thinning to 10 µm. It is estimated that the specific on-resistance of the 10 µm-thick lateral 3C-SiC MOSFETs is 13.3 mΩcm^2 in an active cell area for a blocking voltage of 600 V.

References

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