M-2-3

Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp1281-1282

DC Bias-stress effect for organic thin-film transistors with parylene-C dielectric layers

Kenjiro Fukuda[1], Tatsuya Suzuki[1], Daisuke Kumaki[1] and Shizuo Tokito[1]

[1] Research Center for Organic Electronics, Yamagata University
4-3-16 Jonan, Yonezawa, Yamagata, Japan
Phone: +81-238-26-3594 E-mail: fukuda@yz.yamagata-u.ac.jp

1. Introduction

Organic thin-film transistors (TFTs) have attracted significant attention in research and development for next-generation thin-film electronics because they can be processed on plastic substrates with various printing techniques at very low cost. While recent efforts have achieved significant progress in improving the electrical characteristics of organic TFT devices[1,2], operational stability remains as a major issue to be resolved before organic TFT devices can realize their full commercial potential. The changes in transistor characteristics when applying DC bias stress, hereafter referred to as DC bias stress effects, is the obstacle to long-term operational stability for organic TFT devices, as well as other TFTs including those based on a-Si:H, poly-Si, and metal-oxide semiconductor materials[7-11]. In p-type organic TFT devices, threshold voltage shifts under DC bias stress conditions are generally in a negative direction for negative gate-source voltages[3-5].

In this study we found that organic TFT devices with polychloro-p-xylylene (parylene-C) used for the gate dielectric material exhibited positive threshold voltage shifts under a negative DC gate-source voltage. These shifts increased nearly proportionally with increasing parylene-C layer annealing temperatures. The annealing process improved the crystalline structure of the parylene-C layers, which caused more distinct positive shifts in threshold voltage.

2. Fabrication process

Polycrystalline pentacene TFT devices with parylene-C as gate dielectrics were fabricated by employing a vacuum evaporation process. An illustration of the bottom-gate, top-contact TFT device construction used is shown in Figure 1a. First, aluminum was evaporated onto a glass substrate to form a 50-nm-thick gate electrode. A 500-nm-thick parylene-C (dix-C, KISCO, Figure 1b) layer was then formed by chemical vapor deposition, and was annealed in a nitrogen atmosphere. We prepared several such TFT devices with different annealing temperatures (T_a), ranging from 30 to 150°C for 1 h. Next, pentacene layers were deposited to form a 75-nm-thick organic semiconductor channel on the parylene-C dielectric layers. Finally, gold was deposited to form 50-nm-thick source/drain electrodes. A micrograph of a fabricated TFT device is shown in Fig. 1c. The channel width (W) and the channel length (L) of fabricated TFT devices were 1000 and 65 μm, respectively.

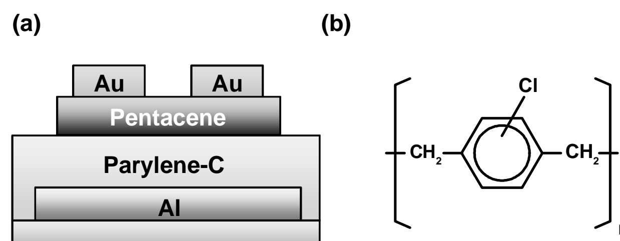

Fig.1 (a) A schematic illustration of the fabricated organic TFT devices with parylene-C as gate dielectrics. (b) Chemical structure for parylene-C.

The DC characteristics of organic TFT devices were measured using a semiconductor parameter analyzer (4200-SCS, KEITHLEY). All the measurements were performed at room-temperature (approximately 25°C) in a nitrogen atmosphere to avoid degradation of fabricated TFT devices in exposure to air[6,7]

3. Results and discussion

Figure 2 shows the change of threshold voltage (ΔV_{TH}) as the devices are stressed with constant bias voltages (V_{GS} = –40 V, V_{DS} = 0 V). Figures 2a and 2b show the changes in transfer characteristics before and after stressing the devices for 3600 seconds, for TFT devices fabricated with anneal temperatures of T_a = 30°C and 150°C, respectively. When a DC gate-source bias voltage of –40 V was continuously applied to the TFTs with annealing temperature Ta = 30°C for 3600 seconds, the threshold voltage shifted slightly in a negative direction from –20.4 V to –20.9 V. Further, when DC bias voltages of –40 V were continuously applied to the TFTs with T_a = 150°C for 3600 seconds,

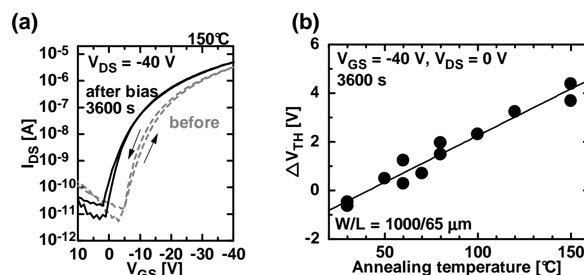

Fig.2 (a) Transfer characteristics for a TFT device with T_a = 150°C taken before and after applying a DC bias voltage (V_{GS} = –40 V, V_{DS} = 0 V) for 3600 secconds. (b) ΔV_{TH} as a function of annealing temperature for the parylene-C layers.

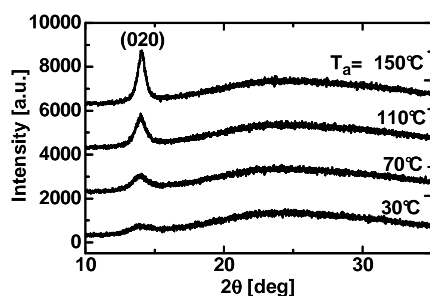

Fig.3 X-ray diffraction patterns from parylene-C thin films with different annealing temperatures. T_a is swept from 30°C to 150°C in 20°C steps.

the threshold voltage shifted dramatically in the positive direction, from –23.6 V to –19.4 V, without changes in other key electrical parameters such as on/off ratio and field-effect mobility. Figure 2c shows $\varDelta V_{TH}$ as a function of stress time. These results demonstrate a strong dependence between threshold voltage shifts and the annealing temperatures for the gate dielectric (parylene-C) layers. This tendency to "reverse" threshold voltage shifts was enhanced with increasing annealing temperatures, T_a. Figure 2b shows $\varDelta V_{TH}$ as a function of T_a, which clearly indicates a linearly proportional change in $\varDelta V_{TH}$ vs. T_a, with the following linear curve fit:

$$\varDelta V_{TH} = 0.041\ T_a - 1.74 \qquad (1)$$

In order to investigate the molecular arrangement of the parylene-C dielectric layers, we analyzed them using X-ray diffraction (XRD). Figure 4a shows the T_a dependence of XRD peak for a parylene-C thin film (layer thickness: 500 nm), such that all measurements were carried out at 30°C. The XRD patterns show that a peak at $2\theta \sim 14.5°$, which is indexed as the (020) crystallographic direction[8], increases with increasing annealing temperature.

There is strong relation between the positive bias stress of TFT devices and the crystallinity of the parylene-C layer. This result indicates that a positive shift in V_{TH} is associated with the presence of dipoles in parylene-C layers[9]. One of the hydrogen atoms in the benzene ring of parylene-C is substituted by a chlorine atom (Figure 1b). The hydrogen atoms have a positive ionic character, while the chlorine atom has a negative ionic character. The XRD results indicate that the parylene-C thin-film layers have amorphous-like crystallinity when the layers are annealed at low temperatures less than 50°C. However, annealing at temperatures over 50°C causes the crystalline growth in the parylene-C layers. The glass-transition temperature (T_g) of 500-nm-thick parylene-C layer is about 45°C[10], This relatively low T_g causes structural re-ordering and then improved crystallinity in the parylene-C layers through annealing. The out-of-plane XRD measurements show that the (020) peak increases through the annealing process, which represents the parylene-C molecular chains stack along the c-axis [11]. Each chlorine atom in a single repeating unit of parylene-C molecule is located randomly upward or downward along the main chain direction when a gate voltage is not applied between gate and source electrodes. When a gate voltage is applied ($V_{GS} < 0$ V), chlorine atoms gradually align upwards by free rotation because of their negative ionic characteristics. The origin of the linear increase in the positive bias shift effect is probably due to the total dipole polarization oriented in the gate-source direction, which increases linearly with increasing the crystallite size through the annealing procedure.

5. Conclusions

In conclusion, we have found that the organic TFT devices with parylene-C layers as gate dielectrics exhibited positive bias shifts under the negative DC gate-source voltages, yet there was almost no hysteresis found in the transfer characteristics. The crystalline domains were aligned and grew via an annealing procedure, which caused the bias shift in the fabricated organic TFT devices to reverse. This tendency to reverse threshold voltage shifts under the DC bias voltage could potentially be useful in controlling TFT devices with stable bias.

Acknowledgements

The authors would like to acknowledge the Japan Science and Technology Agency (JST) for their support of this work.

References

[1] H. Minemawari, T. Yamada, H. Matsui, J. Tsutsumi, S. Haas, R. Chiba, R. Kumai, T. Hasegawa, Nature 2011, 475, 364-367.
[2] R. Schmidt, J. H. Oh, Y. Sun, M. Deppisch, A. –M. Krause, K. Radacki, H. Braunschweig, M. Konemann, P. Erk, Z. Bao, F. Wurthner, J. Am. Chem. Soc. 2009, 131, 6215-6228.
[3] T. Sekitani, S. Iba, Y. Kato, Y. Noguchi, T. Someya, T. Sakurai, Appl. Phys. Lett. 2005, 87, 073505.
[4] A. Salleo, F. Endicott, R. A. Street, Appl. Phys. Lett. 2005, 86. 263505.
[5] H. L. Gomes, P. Stallinga, F. Dinelli, M. Murgia, F. Biscarini, D. M. de Leeuw, T. Muck, J. Geurts, L. W. Molenkamp, V. Wagner, Appl. Phys. Lett. 2004, 84, 3184-3186.
[6] K. Fukuda, T. Sekitani, T. Someya, Appl. Phys. Lett. 2009, 95, 023302.
[7] T. Sekitani, S. Iba, Y. Kato, Y. Noguchi, T. Someya, T. Sakurai, Appl. Phys. Lett.
[8] M. C. Demirel, S. Boduroglu, M. Cetinkaya, A. Lakhtakia, Langmuir 2007, 23, 5861-5863.
[9] D. K. Hwang, M. S. Oh, J. M. Hwang, J. H. Kim, S. Im, Appl. Phys. Lett. 2008, 92, 013304.
[10] H. L. Huang, Y. Xu, H. Y. Low, Polymer 2005, 46, 5949-5955.
[11] S. Isoda, T, Ichida, A. Kawaguchi, K. Katayama, Bull. Inst. Chem. Res., Kyoto Univ. 1983, 61, 222-228.