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It is a small world

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1. Abstract

Our expanding information infrastructure is growing to form super networks of data centers, smart mobile devices, and sensor networks. This growth will demand a variety of energy-efficient electronic systems that can satisfy a myriad of performance, form-factor, and cost needs. Thus giving rise to new drivers for performance and density scaling of logic and memory contents of the chips.

Since the early part of this decade, the industry has transitioned from a mostly lithographically-reliant transistor shrink to a “Post-Dennard” era that also relies on new material for performance scaling. The pace of new material and device structure innovations has not slowed since. This process-complexity trend has been common to both logic and memory devices. Logic devices have evolved from poly-SiON gate to High-k Metal gates, to be followed by fully-depleted channel devices for 22nm logic and beyond. While new memory devices like RRAM and STT-MRAM are emerging as embedded storage solutions, potentially complementing/replacing the future SRAM and DRAM contents on the chip.

The scaling for the next decade may evolve through another inflexion, where functionality and performance are dramatically stepped up through reliance of multi-level heterogeneous integration, that starts from transistors and continues to logic, memory, system-on-chip levels To build the superchips of tomorrow, novel interconnects, 3-D, and 2-D co-integration will be needed. By examining the technology drivers and challenges, we will discuss how the logic and memory device roadmaps are being shaped to support the new super-chip vision for 15nm CMOS and beyond. Imec’s logic scaling roadmap is shown in Fig 1.

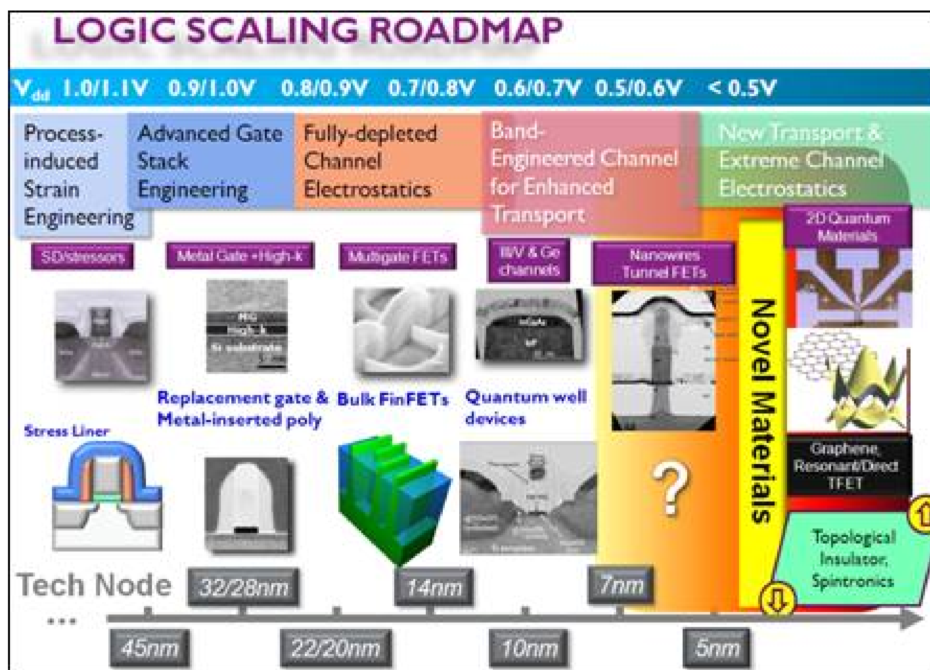

Fig. 1 Imec Logic Device Roadmap

2. CMOS 14 nm

Gate-stack scaling of EOT alone can no longer address the transistor electrostatic scaling needed for 14nm technology, especially for low-Vdd (0.8V) performance. Fully-depleted channel devices with improved electrostatics, like bulk FinFET/Multi-gated (MUGFET) devices, are being investigated as front-up options in combination with the next generation replacement metal gate (RMG) module. The RMG material is the key to control the FinFET Vt. A SiGe channel is one of the candidates to manage PFET device characteristics.

3. CMOS 10 nm

Targeting 10nm, energy-band-engineered quantum-well and high-mobility channel materials are being investigated. Alternate to Si, III-V , Ge, SiGe channel materials are being looked into for sub-0.8V V_{dd} technologies. The material path-finding activities focus on the material development, integration, and defect mitigation for device enablement. Among the approaches is the study of Aspect-Ratio-Trapping (ART) epitaxial channel growth in trenches. Gate-stack and channel passivation to minimize the electrical impact of traps are of top focus also. To address the need for mobility enhancement, work to assess the extendibility of process-induced stressor for 10nm devices are being performed. In addition, new material (Eg. GeSn) and process strain engineering are being looked into as well. The goal is to identify promising process options and associated layout rules, ready for platform-level experiments.

4. CMOS 7nm and beyond

For 7nm and beyond, novel devices with high-confinement electrostatics (Eg. Nanowires) and new transport (Eg. Tunneling FETs(TFETs)) are being investigated. The goal is to look into devices that provide improved performance and variability for sub-0.7V Vdd operations. The approaches here are not only to extend mobility enhancement for drive current increase, but look into sub-threshold enhancement to effectively increase I_{on}/I_{off} ratio, especially for low V_{dd} operations. For TFETs, work is invested to understand how to overcome the diffusion limit to sub-threshold swing of 60mV/dec by utilizing quantum-mechanical tunnel operation. In the case of nanowires, the approach is to maintain short-channel electrostatics as close to long-channel sub-threshold swing, while minimizing parasitic and maximizing drive. In support of 7nm-and-beyond research, emerging highly-ordered 2-D materials that may enable device performance and electrostatics are being researched as well. These include single and bi-layer graphene. The first objective here is to study the properties of these materials to engineer band gap, effective carrier masses, and novel transport.

5. Variability and process control

Variability is a growing influence and detractor to scaling. With new devices, new materials, diminishing feature sizes, and increasing system complexities come new sources of variability and new sensitivities.

Examples of non-time-varying / slow-varying sources of variation are Random Doping Fluctuation (RDF), Process Variation, Mismatch etc. But also time-varying sources are growing, such as BTI (Bias Temperature Instability) and temperature variation. For slow-varying sources there are emerging system-level adaptations possible. The most challenging ones the fast-changing ones at the transistor level and below like noise, where only device and material innovations can address.

6. Process complexity and cost

Process complexity has and will drastically increase for the advanced CMOS nodes. Cost management will be a crucial factor going forward. One example is the usage of EUV lithography to replace multiple patterning using 193i lithography. Another possibility might be system scaling by die stacking enabled by 3D TSV (Through-Silicon-Via) technology. The question is still out there if this can at one point become more cost effective than lithography scaling. And last but not least, lowering the cost by upscaling the wafer size. The traditional rate of cost reduction per transistor cannot be maintained without a wafer scale up approx every 10 years.

7. Conclusions

In summary, Moore's law continues ... driving to sub-15nm dimensions where EUV lithography will be a necessity. Another trend in CMOS scaling is the migration to 3D device architectures (FinFET) with advanced material innovation around high-mobility channel materials. The increase in process complexity and variability requires early technology / design co-optimization.

8. Acknowledgements

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