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One-step Further of Wide Band-gap Semiconductor SiC

Hiroyuki Matsunami

Kyoto University
1-9 Nishiyama-adachi, Yawata-city, Kyoto
phone: +81-75-981-7341 Email: h_matsunami@kcat.zaq.ne.jp

1. Introduction

Silicon carbide (SiC) has superior properties such as wide band-gap, high breakdown field strength, high saturation electron drift velocity, and high thermal conductivity. Using such superior properties, SiC power devices have much higher performance such as low-loss, high switching speed, high-temperature operation and simple cooling system compared to ordinary Silicon (Si) power devices. Though we hold out great hopes for SiC as a power semiconductor material, it has taken a long time to develop this material.

In this presentation, after brief history, the progress in SiC technology: such as bulk crystal growth, epitaxial growth, processes, and majority carrier devices below 5 kV rating as blocking voltage, together with remained problems are described. Above 5 kV, minority carrier devices will take the position utilizing conductivity modulation, and recent progress on those devices is introduced as one-step further SiC power devices.

2. Brief History

The author's group proposed a new technology named "step-controlled epitaxy" for high-quality SiC epitaxial layer in the late 80's [1]. The use of off-axis (0001) substrates is a key idea to obtain high-quality epitaxial layers at rather low substrate temperatures utilizing step-flow growth. We elucidated the growth mechanism in "step-controlled epitaxy", and characterized epitaxial layers and performed conductivity control, which were reviewed in the literature [2]. Being stimulated by this breakthrough, the opportunity to use SiC for power devices grew ripe in the middle of 90's. We demonstrated high-voltage SiC Schottky barrier diodes in 1993 [3], and 1995 [4], which were commercialized in 2001. Power Schottky barrier diodes (SBDs), junction field-effect transistors (JFETs), and metal-oxide-semiconductor field-effect transistors (MOSFETs) have been developed, and are now on the market.

3. Crystal Growth and Processes

bulk growth

For bulk crystal growth, a seeded sublimation technique (modified Lely method) [5] has been widely used, and nowadays 4-inch diameter wafers are commercially available. The reduction of various dislocations such as screw, edge, and basal plane dislocations has been extremely carried out. By using a unique technique of Repeated A-face Growth (RAF) method [6], the dislocation density has been reduced by almost 2 orders of magnitude, and this technique is now being developed for usable production. Bulk crystal growth to get 6-inch diameter started.

Epitaxial growth [2]

Step-controlled epitaxial growth has been studied deeply, and now almost all epitaxial layers are grown on off-axis substrates by chemical vapor deposition using a SiH_4-C_3H_8-H_2 system. The impurity concentration of undoped layers is in 10^{12}-10^{13} cm^{-3} by control of C/Si ratio. For n-type, the density of donors is controlled up to 10^{19} cm^{-3} using N_2 gas, and for p-type, the density of acceptors up to $10^{20}cm^{-3}$ using TMA (trimethylaluminum).

Ion implantation [7]

Ion implantation is important for selective doping. Hot (or warm) implantation is effective to recover crystal quality. For n^+-SiC, a low sheet resistance of 290 Ω/□ and 51 Ω/□ can be obtained using high-dose N or P, respectively. For p^+-SiC, still a high sheet resistance of 3-8 kΩ/□ is obtained, though high-dose Al is used. High-temperature annealing at 1600-1700℃ is necessary to get higher activation ratio than 90%. It causes a roughened surface, which may affect device performance. A graphite cap is most useful in the process.

Thermal oxidation [7]

For the fabrication of MOSFETs, thermal oxidation in a wet or dry atmosphere results in residual carbon in the oxide and carbon clusters at the SiO_2/SiC interface. Carbon-cluster related centers are responsible for donor states in the lower part and for continuous states in the central part of the band-gap. Acceptor-type defects in the upper part of the band-gap are likely related to intrinsic oxide defects: O-deficiency. Post oxidation annealing in nitrogen containing atmosphere such as nitric oxide (NO) or nitrous oxide (N_2O) is effective for lowering interface state densities.

Ohmic contacts [7]

The most promising material is Ni for n-type with $3.3x10^{-7}$ Ωcm^2 and Al-Ti for p-type with $9.7x10^{-7}$ Ωcm^2 by optimization of surface pretreatment of highly-doped ($>10^{19}cm^{-3}$) layer followed by post deposition annealing. Long-term stability of ohmic contacts at 500℃ was reported.

4. Unipolar Devices (Majority Carrier Devices) [8]

SBDs

High performance of high-voltage 4H-SiC SBDs was demonstrated in 1995 [4], followed by excellent reverse characteristics of high-voltage SBDs with boron-implanted edge termination. Based on many efforts, SBDs with blocking voltages of 300-1,700V and current rating of 6-20 A are commercially available. SBDs of 600-3,000 V and 80-300 A are now on research and development (R&D) stages for sample delivery.

JFETS

Vertical junction field-effect transistors (VJFETs) have been commercialized after SBDs. Although JFETs are normally-on type, the main current flow path is not influenced by interfaces between SiC and insulators as in MOSFETs. For normally-off type operation, the combination of low-voltage Si MOSFET and high-voltage SiC JFET (cascode principle) is commercially available.

MOSFETs

Mass production of vertical MOSFETs (DMOSFETS: double-implanted MOSFETs and UMOSFETs (or trench MOSFETs) started and now in commercial base. Still, important problems of MOS interface remained, such as low channel mobility and reliability. Recent progress in this area such as (ⅰ) effects of nitridation, (ⅱ) thermal oxidation vs. deposited oxide, (ⅲ) channels on different crystal planes, and (ⅳ) reliability will be described from scientific and technological points of view.

5. Bipolar Devices (Minority Carrier Devices) [8]

For above several kV as blocking voltage in the application to electric power infra-structure and smart grid, minority carrier devices such as pin diodes, bipolar transistors (BPTs), gate turn off thyristors (GTOs), and insulated gate bipolar transistors (IGBTs) will take the position. In this area, R&Ds have been carried out, but those devices are not in commercial stages.

For one-step further, scope and scheme of fundamental research program in Japan will be overviewed. Important subjects are minority carrier lifetime in epitaxial layers, junction termination enhancement (JTE), and surface passivation. Some of recent results such as (ⅰ) quality of thick epitaxial layers grown with high growth rate, (ⅱ) correlation of minority carrier lifetime with carbon vacancy, (ⅲ) improvement of carrier lifetime by thermal annealing, (ⅳ) structure of JTE, (ⅴ) surface passivation to avoid leakage and discharge at ultra high-voltage will be discussed. Examples of ultra high-voltage pin diodes with blocking voltage above 20 kV will be presented.

5. Summary

To realize high-performance SiC power devices, various approaches are taken from scientific and technological points of view. Unipolar devices are now in the market and usefulness of those devices has been reported. To overcome ultra high-voltage, bipolar devices are in R&D stages. Reviews on established subjects and challengeable ones are presented.

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References

[1] N. Kuroda, K. Shibahara, W.S. Yoo, S. Nishino and H. Matsunami, *Extend. Abstr. 19th Conf. on Solid State Devices and Materials*, Tokyo, 1987, p.227.

[2] H. Matsunami and T. Kimoto, Mater. Sci. & Eng., **R20** (1997) 125.

[3] T. Kimoto, T. Urushidani, S. Kobayashi and H. Matsunami, IEEE Elec. Device Lett., **14** (1993) 548.

[4] A. Itoh, T. Kimoto and H .Matsunami, IEEE Elec. Device Lett., **16** (1995) 280.

[5] Yu.M. Tairov and V.F. Tsvetkov, J. Cryst. Growth, **43** (1978) 209.

[6] D. Nakamura, I. Gunjishima, S. Yamaguchi, T. Ito, A. Okamoto, H. Kondo and K. Takatori, Nature, **430** (2004) 1009.

[7] H. Matsunami, Jpn. J. Appl. Phys., **43** (2004) 6835.

[8] P. Friedrichs, T. Kimoto, L. Ley and G. Pensl eds., *Silicon Carbide*, Wiley-VCH, Vol. 2, 2009.