Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp30-31

Double-Gated Junctionless Vertical Channel Poly-Si Thin-Film Transistors

Yi-Hsuan Chen, Je-Wei Lin, Li-Chen Yen, Rou-Han Kuo, Yi-Hsien Lu, Yi-Hong Wu, Po-Yi Kuo, Tien-Sheng Chao

Department of Electrophysics, National Chiao Tung University,
1001 Ta Hsueh Rd, Hsinchu, Taiwan
Phone: +886-3-5131367 Fax: +886-3-5725230 E-mail: HopTrains@gmail.com

1. Introduction

In recent years, the concept of junctionless metal-oxide-semiconductor field-effect transistors (MOSFETs) has attracted considerable attention. However, most of the JL devices utilize a nanowire (NW) structure as the channel. Although devices with NW channels have shown excellent performance [5], fabrication processes of NW devices are much more complicated than that of planar ones. In this work, we propose a double-gated, junctionless vertical channel thin-film transistor (DG JL-VTFT) and first demonstrate that the concept of JL MOSFETs can be realized on **v**ertical channel **t**hin-**f**ilm **t**ransistor (VTFT). VTFT has great potential for gate length scaling since its gate length is determined by the thicknesses of the deposited film and thus does not require advanced photolithography equipment or etching processes. An ultra-thin channel was used to sustain enough on/off ratio, and Ni-salicidation was utilized to maintain acceptable drive current. The temperature dependence of transfer characteristics and the influence of plasma treatment on device performance were also studied.

2. Experiment

Fig. 1 (a) to (e) show the process flow and schematic cross-sectional view of the DG JL-VTFTs without Ni-salicidation. First, silicon wafers were covered with 550-nm-thick thermal oxide as the glass substrate and 200-nm-thick poly-Si thin film as the gate by low-pressure chemical vapor deposition (LPCVD). The gate (or bottom gate) was implanted with BF_2 (70 keV at 5×10^{15} cm^{-2}) and activated at 600°C for 12 h in N_2 ambient. After gate patterning, the wet-oxide was overetched to form the offset region. Tetraethoxysilane (TEOS) oxide and *in-situ* phosphorous doped poly-Si were then deposited sequentially as the gate oxide and active region by LPCVD. After the active-region patterning, another TEOS oxide and poly-Si were deposited sequentially as the gate oxide and top gate. The top gate was implanted with BF_2 (70 keV at 5×10^{15} cm^{-2}) and activated at 600°C for 12 h in N_2 ambient. Ni-salicidation were formed on some of the samples after top gate patterning.

3. Results and Discussion

In our experiment, a vertical channel thin-film transistors without junctions and the top gate (called SG JL-VTFT) are also fabricated for comparison with DG JL-VTFTs. Fig. 2 shows across-sectional transmission electron microscope (TEM) micro-photograph of a DG JL-VTFT.

Fig. 3 presents the transfer characteristics of both SG and DG JL-VTFTs in which $W/L_{floating}$ = 1/1 μm. The SG JL-VTFTs shows higher on current, but cannot effectively turn off. According to the TEM (Fig. 2), the channel film thickness of the DG JL-VTFTs is slightly smaller than the SG JL-VTFTs due to an additional cleaning process before TG oxide deposition [6]. Therefore, the drain current is also degraded because of the reduction of the conductive area and increase of the resistance. The transfer characteristics of the DG JL-VTFTs with different operation scheme are shown in Fig. 4. As expected, the JL-VTFTs with double gate control performs better than ones only with either top gate or bottom gate sweep by presenting higher on current and steeper subthreshold swing.

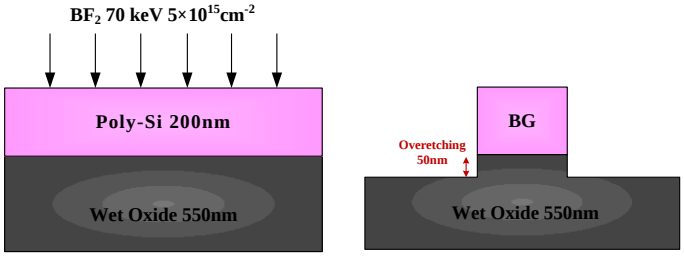
To further enhance the performance, we use metal-salicidation technology to improve the drain current. Fig. 4 shows the transfer characteristics of the DG JL-VTFTs with and without Ni-salicidation. Fig. 6 shows the transfer characteristics of DG JL-VTFTs with Ni-salicidation under various temperatures. As temperature is increased, the threshold voltage decreases, and the subthreshold slope (SS) and off-state leakage current increase. In addition to Ni-silicidation, the performance of DG JL-VTFTs may also be enhanced by NH_3 plasma treatment Fig.7. With optimized period of plasma treatment, SS can achieve 350 mV/dec, and on/off ratio can exceed 6 order.

Conclusion

In this paper, we have successfully fabricated and demonstrated junctionless, double-gated vertical channel poly-Si thin-film transistors. The channel film thickness is a very important factor in the carrier transport. Hence, it is important to trade off the channel film thickness to obtain optimum device characteristics. The drain current can be improved using Ni-salicidation technology. The threshold voltage decreases as temperature is increased. The subthreshold slope, off-state leakage current and on-state current increase as temperature increases.

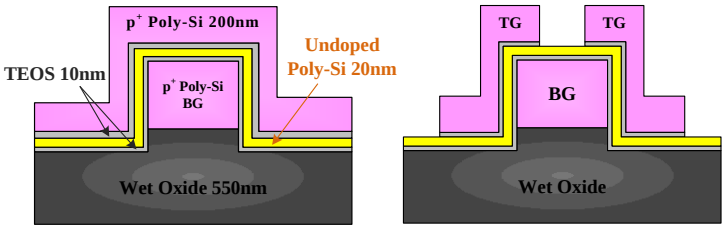
References

[1] J. P. Colinge *et. al.* , Nat. Nanotechnol. **5** (2010) 225.
[2] C. W. Lee *et. al.* , Solid-State Electron., **54**(2010) 97.
[3] C. W. Lee *et. al.* , Appl. Phys. Lett. **94** (2009) 053511-1.
[4] C. J. Su *et. al.* , IEEE Electron Devices Lett. **32** (2011) 521.
[5] H. C. Lin *et. al.* , IEEE Trans. Electron Devices **53** (2006) 2471.
[6] C. M. Lee *et. al.* , IEEE Electron Device Lett. **31** (2010) 683.



(a) Wet oxide / poly-Si deposition and gate implant

(b) gate patterning and offset region overetching



(c) BG oxide / channel / TG oxide / TG deposition

(d) BG oxide / channel / TG oxide / TG deposition

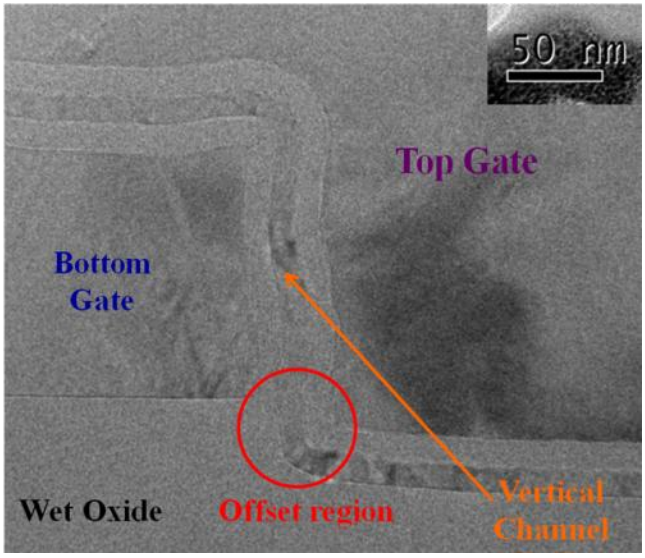
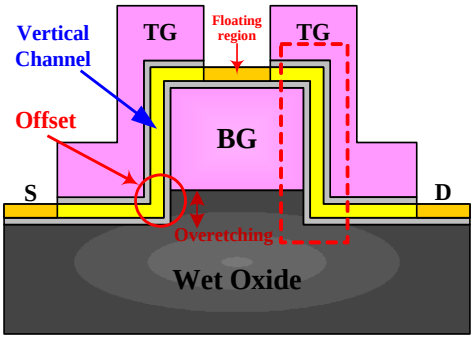


Fig. 2 Cross-sectional transmission electron microscope (TEM) micro-photograph of DG JL-VTFTs (range is the rectangle of red dashed line in Fig. 1) .



(e) cross-sectional diagram

Fig. 1 (a)-(d) show the process flow of DG JL-VTFT and (e) presents the schematic cross-sectional diagram of DG JL -VTFT without Ni-salicidation.

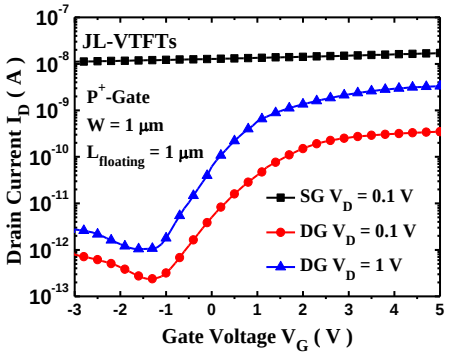


Fig. 3 Transfer characteristics of SG JL-VTFTs and DG JL-VTFTs with $W/L_{floating}$ = 1/1 m

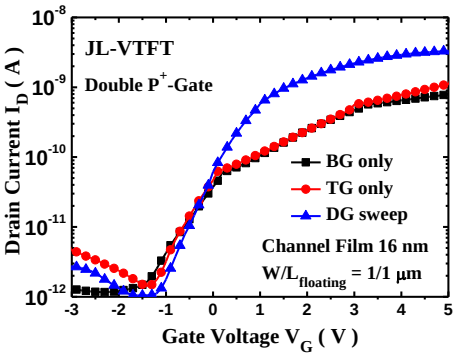


Fig. 4 Transfer characteristics of DG JL-VTFTs with different operation scheme.

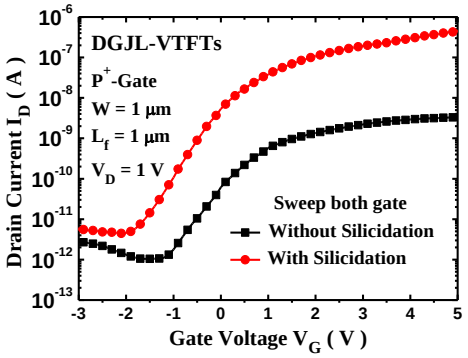


Fig. 5 Transfer characteristics of DG JL-VTFTs with and without Ni-salicidation.

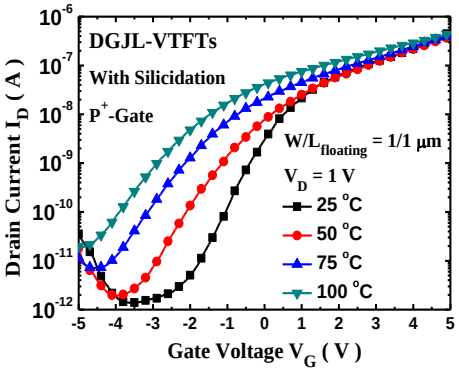


Fig. 6 Transfer characteristics of DG JL-VTFTs with various temperatures.

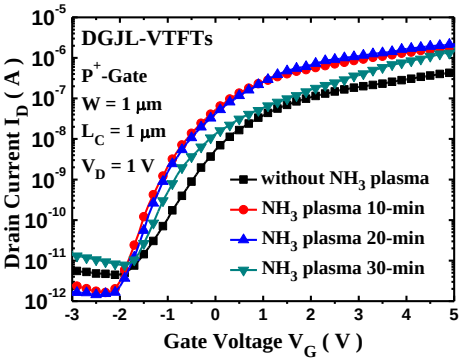


Fig. 7 Transfer characteristics of DG JL-VTFTs with or without NH_3 plasma treatment.