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Multi-Step Deposition and Low-Temperature Two-Step (Ultraviolet Ozone cum Rapid Thermal) Annealing as a Promising Means for Gate-Last High-k/Metal Gate Application

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1. Introduction

The gate-last integration scheme is gaining increasing attention due to its advantage in overcoming issues such as undesirable increase in the interfacial layer (IL) thickness and high-k crystallization[1]. However, due to the constraint of low thermal budget process, the conventional rapid thermal (typically in high temperature ~600 ºC and above) treatment on the structural defects (i.e., oxygen vacancy, V_O) in high-k film is no longer suitable[2]. Therefore, it is essential to find a means for reducing the V_O density through proper deposition and treatment in a low thermal-budget process in order to enhance electrical performance. In this work, we demonstrate a *two-step* annealing approach for enhancing the quality of high-k dielectric in a gate-last process. In particular, a gate stack annealed with UV-O_3 followed by a 420 °C rapid thermal (RTA) exhibits (i) an evident reduction in the gate leakage current density (J_g), and (ii) improved breakdown (BD) strength without EOT penalty.

2. Experimental Details

An intentional 1.5-nm thermal oxide was formed on a p-Si substrate, followed by the atomic layer deposition of a 2.8-nm HfO_2 at 250-°C. The HfO_2 was deposited and annealed in four steps. In each step, an ultrathin 0.7-nm HfO_2 was subjected to room-temperature UV-O_3 anneal for 1 min followed by RTA at 420-ºC for 30 s in N_2 (Fig. 1). The order of the two-step anneal was reversed (i.e., RTA precedes UV-O_3) for some samples to assess the effect on the electrical characteristic of the gate stacks. In some cases, either the UV-O_3 or the RTA was omitted to study the relative impact of each annealing step. The respective gate stacks are denoted as UVO-RTA, RTA-UVO, RTA and UVO. For reference, as-deposited (as-dep) HfO_2 was grown under exactly the same conditions as the four-step deposited samples, but with both the UV-O_3 and RTA anneal skipped. The STM study was performed on the blanket-deposited samples in ultra-high vacuum (~10^{-10} Torr) under controlled temperature. The bias voltage V_s was applied to the p-Si and the STM probe (Pt/Ir) was grounded. On some samples, TiN was sputtered and patterned to form MOS capacitors before subjected to forming gas anneal at 425 °C for 30 min. For comparison with a gate-first process, one of the as-dep HfO_2 was exposed to source/drain activation anneal (~1000-°C for 5 s in N_2) after TiN gate formation.

3. Results and Discussion

A. *STM-measured Topography and Current Maps*

Fig. 2(a) shows the constant-current topography images of the various HfO_2 gate stacks. Granular features are evident in the RTA (1000-°C) sample, implying that the HfO_2 has crystallized[3]. The low conductivity grain regions (denoted by the bright shades in the topography) are clearly surrounded by the "leaky" grain boundaries (denoted by the bright shades in the corresponding current map in Fig. 2(b)(i)). Such features, however, are not apparent in the as-dep (Fig.2 (ii)) and those low-temperature annealed (Fig. 2(iii) to 2(vi)) samples. In these samples, the HfO_2 exhibits an amorphous-like structure. Compared to the as-dep sample, the bright shade density, arising from defects, in the current maps of both the RTA and UVO samples are clearly reduced. This may be attributed to film densification and V_O "repair", respectively, by the RTA and UV-O_3 anneal. A further reduction is achieved for the two-step annealed samples. It is believed that the combined effect of RTA and UV-O_3 yields a more efficient V_o "repair".

B. *I-V and C-V Characteristics*

The reduction in the density of leakage sites depicted in Fig. 2(b)(i) to 2(b)(vi) is in agreement with the corresponding lowering of the average tunneling current (I_t) spectra and the reduced statistical spread of I_t as shown in Fig. 3 and Fig. 4 respectively. Fig. 5(a) shows the quasi-static high-frequency capacitance versus gate voltage (V_g) characteristics. Compared to the as-dep samples, those samples annealed (irrespective of single-step or two-step) in UV-O_3 exhibit a more positive flat band voltage (V_{FB}), indicating a reduced density of positive oxide trapped charge. An almost identical V_{FB} shift between the UVO and the RTA-UVO samples implies that the preceding RTA of the later has little effect on the V_{FB}. It is interesting, however, to note that a further positive V_{FB} shift is achieved for the UVO-RTA sample, implying further removal of V_O's by the 420-°C RTA carried out after the UV-O_3 anneal. The EOT of all the gate stacks are almost identical, indicating that the multi-step deposition and two-step anneal retain overall gate stack thickness (Fig. 5(b)). The larger EOT of the RTA(1000-°C) gate stack may be ascribed to an increase of the interfacial oxide layer thickness[4]. Fig. 6(a) shows the corresponding gate current density J_g versus V_g curves. A large J_g and small BD voltage V_{BD} is observed for the 1000-°C RTA gate stack as a result of a crystallized HfO_2. Compared to the as-dep gate stack, the J_g of the 420-°C RTA and UVO sample are reduced by about an order of magnitude in the low V_g regime. The improvement in J_g is attributed to the removal of carbon-related impurities and V_o "repair" respectively. A further reduced J_g is achieved for RTA-UVO sample, indicating a more efficient V_o "repair" by UV-O_3 after the removal of impurities by the preceding 420 °C RTA. However, as the order of the two anneals is reversed, i.e., UV-O_3 precedes 420 °C RTA, the J_g is further reduced. A plausible explanation is that the RTA, when carried out after UV-O_3, not only removes the impurities but also provides thermal activation which improves V_o "repair". Fig. 6(b) depicts J_g as a function of EOT in comparison to the poly-Si/SiO_2 benchmark.

C. *Gate Stack Breakdown and Stress-induced Degradation*

The BD strength of the gate stacks are evaluated by subjecting to a constant V_g (–4.8 V) stressing at 125 °C (Fig. 7(a)). The T_{BD} of the two-step annealed samples is observed to be significantly improved. UVO-RTA sample, in particular, shows ~5 and ~14 times longer T_{BD} compared to that of the RTA-UVO and as-dep samples respectively. This result clearly shows that the two-step anneal evidently enhanced the BD strength of a gate stack and the order of the two-step anneal is important for achieving a greater improvement. An almost identical Weibull slope of the statistical distributions of the respective gate stacks indicates a similar degradation mechanism governing the BD. In addition, the two-step annealed samples exhibit less susceptibility to stress-induced positive trapped charge generation compared to the single-step annealed samples, as evidenced by a smaller V_{FB} shift under negative constant V_g (–4.4 V) stressing (Fig. 7(b)). The UVO-RTA sample, which shows the smallest V_{FB} shift, corresponding to a better resistance to trapped charges generation, indicates that this annealing order is most effective in V_o "repair" for enhancing the quality of a high-k film.

4. Summary

This study demonstrates a promising two-step (i.e., UV-O_3 followed by RTA) annealing method for enhancing the HfO_2 film quality in a gate-last CMOS process. The trap generation of the HfO_2/IL gate stack formed via multi-step deposition and two-step annealing was studied and compared with those subjected to one-step annealing. An improved BD characteristic is clearly observed for the two-step annealed high-k stack, particularly the UVO-RTA gate stack. It is believed that the RTA plays an important role which enhances the "repair" of V_o-induced traps.

References [1] Packan *et al.*, IEDM 2009, 659-662; [2] Cartier *et al.*, IEDM 2006, 57-60; [3] Yew *et al.*, J. Electrochem Soc. (158), H1021-H1021 (2011); [4] Lee *et al.*, APL (76), 1926-1928 (2000); [5] Ong *et al.*, APL (92), 022904 (2008).

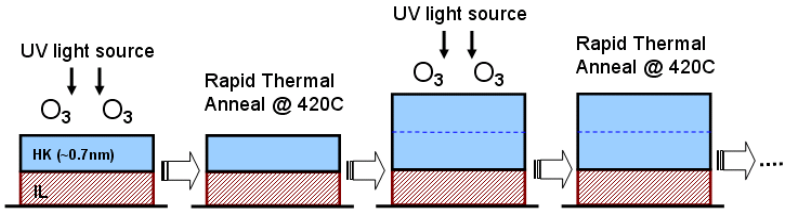

Fig. 1. Schematic illustrations of the UVO-RTA gate stack deposition process. An ultrathin (~0.7-nm) HfO_2 layer is grown via ALD and subsequently subjected to room-temperature UV ozone anneal for 1 min follows by RTA at 420 ºC for 30 s in N_2. This process is repeated until the final thickness is achieved.

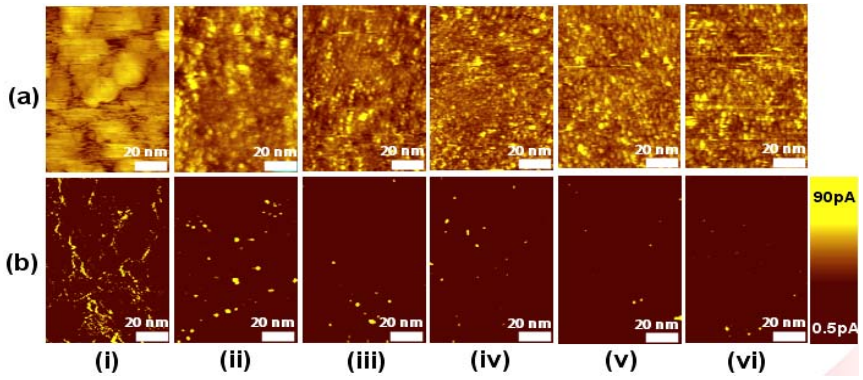

Fig. 2. Row (a) shows the constant-current topography images of the (i) RTA1000ºC, (ii) as-dep, (iii) UVO, (iv) RTA, (v) RTA-UVO, and (vi) UVO-RTA HfO_2 gate stacks acquired at V_s= 2.5 V and I_t= 15 pA. Row (b) shows the corresponding current maps (at V_s = –3 V). Bright shades denote regions of higher I_t. The scanned area: 100 x 100 nm^2.

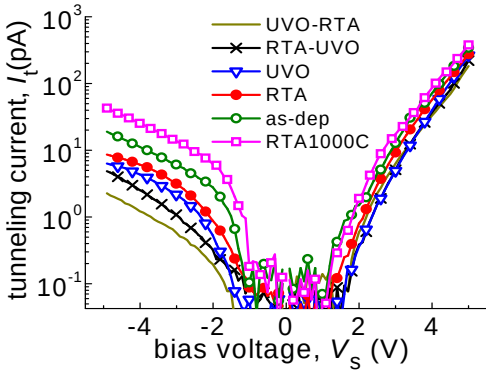

Fig. 3. The corresponding average *I-V* curves extracted from the 100 x 100nm^2 scanned area depicted in Fig. 2(b). Bias voltage V_s was swept from 5 to −5 V. I_t is normalized to the value at 5 V.

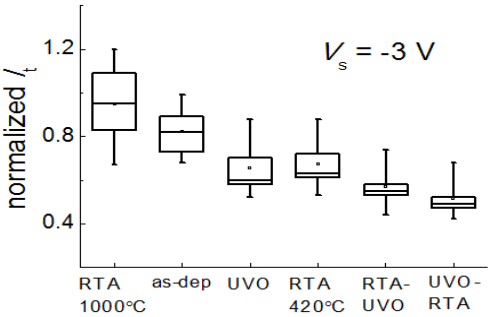

Fig. 4. The corresponding statistical spread in the I_t of the 100 × 100 nm^2 scanned area depicted in Fig. 2(b). I_t is normalized to the average value of the RTA1000 °C sample. The I_t is measured under substrate injection biasing, V_s = -3 V (probes traps in the IL[5])

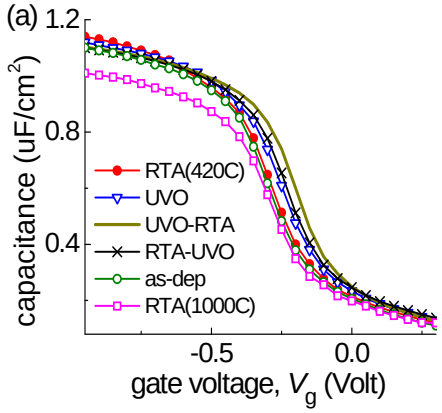

Fig. 5. (a) Quasi-static high-frequency *C-V* characteristics of the HfO_2 gate stacks subjected to various annealing conditions. (b) An almost identical equivalent oxide thickness (EOT) for all the samples except for the one annealed at 1000 °C.

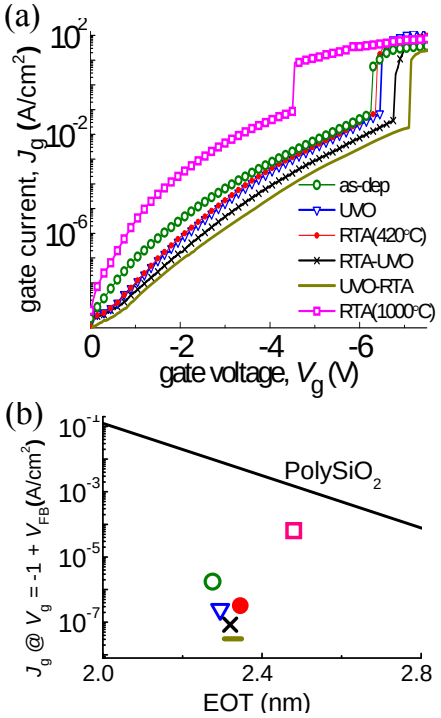

Fig. 6. (a) Gate current density J_g of the various gate stacks measured under room temperature (300 K). (b) J_g versus EOT of the gate stacks. The theoretical data for the poly-Si/SiO_2 gate stack is shown as reference.

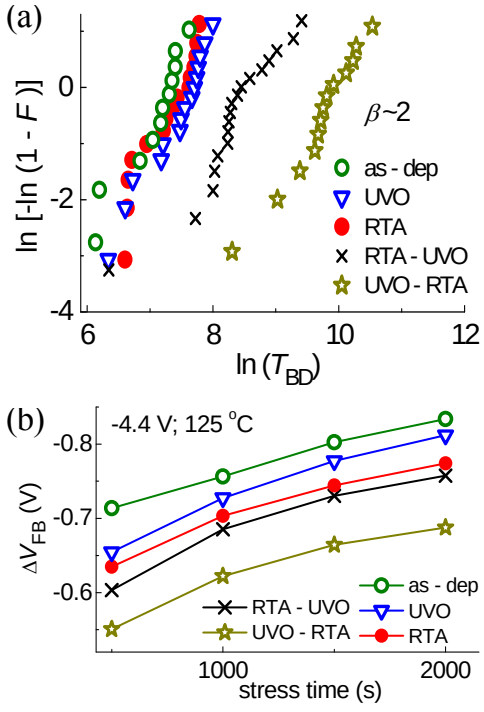

Fig. 7. (a) Time-to-breakdown T_{BD} distribution of the various gate stacks subjected to constant gate voltage (–4.8 V) stressing at 125 °C. Capacitor area: 50 × 50 μm^2. (b) Flat band voltage shift ΔV_{FB} as a function of stress time under constant gate voltage stressing (-4.4 V) at 125°C.