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Low-Temperature Formation of High-Quality Oxide for MOSFETs on Flexible Substrates

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1. Introduction

Silicon dioxide is the most reliable dielectric material to be used in MOSFETs. Although the TFTs have been successfully made and integrated in the flexible electronics, TFTs must be further improved to be operated in the normal-off mode with thin gate dielectric. For this purpose, high-quality gate oxide must be deposited on Si or semiconductor at temperature low enough not to damage a plastic substrate. We reported high-quality oxide formed at 400 ^{o}C by evaporation of SiO nanopowder and post UV oxidation and obtained a midgap interface state density of 1 x 10^{12} cm^{-2}eV^{-1} for the MOS capacitor with gate oxide formed on Si at 200 ^{o}C [1]. Although the interface state density of the MOS capacitor with gate oxide formed at 400 ^{o}C was 6 x 10^{10} cm^{-2}eV^{-1}, as low as that for thermally grown oxide, the interface state density for 200 ^{o}C was still too high. In this paper we report the further decreased interface state density by optimizing the post UV oxidation.

2. Experimental

The disk cut from the pellet formed by pressing the SiO nanopowder was placed in a PBN crucible of the Knudsen-cell, which was heated at 1,000 ^{o}C in the vacuum chamber with a base pressure of 10^{-5} Pa. The thickness estimated form the deposition rate was 30 nm. The post UV oxidation was carried out for 2 hrs by irradiating the deposited oxide with the UV light from a metal halide lamp source (wavelength 250 – 400 nm, power 600 mW/cm^2) in dry or wet oxygen atmosphere, which was formed by filling the chamber with O_2 or O_2 through the bubbler with water heated at 100 ^{o}C. In the wet oxidation, the chamber wall was heated to keep steam from condensing into water. The substrate temperature was kept at 200 ^{o}C during the UV oxidation. The electrodes with a diameter of 300 μm were deposited in vacuum, and then annealed in a flow of forming gas at 200 ^{o}C for 20 min. The high-frequency and quasi-static C-V measurements were made with an Agilent 4282A at 1 MHz and a Keithley 595, respectively. The interface state density was calculated from the high-frequency and quasi-static C-V curves. The stoichiometry of the SiO_x films was evaluated from the frequency of the Si-O-Si stretching vibration measured using an FTIR spectroscopy (Shimadzu FT-IR 8400S) with a reference of thermally grown oxide.

3. Results and Discussion

Figure 1 shows the FTIR spectra of the UV-oxidized

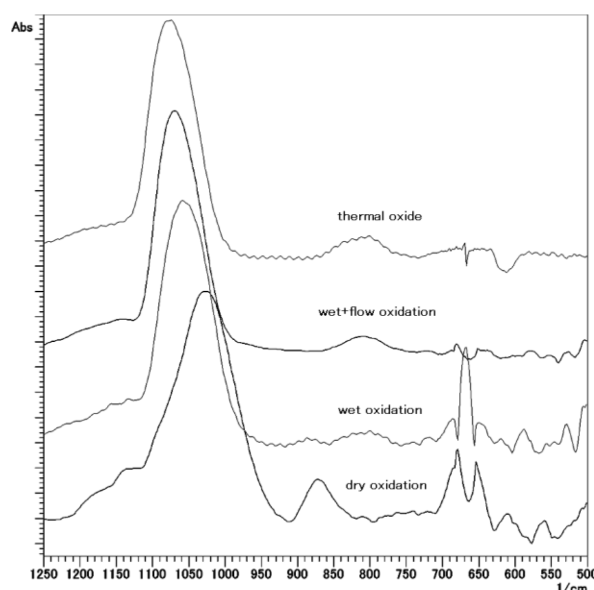

Fig. 1 FTIR spectra of the UV-oxidized SiO_x sampels.

samples under the wet and dry conditions. The FTIR spectrum of thermal oxide is also shown in the figure. It is well known that the frequency of the Si-O-Si stretching vibration monotonically increases with the oxygen atom concentration and reaches 1,078 cm^{-1} in stoichiometric SiO_2 [2]. The oxide film formed by wet UV-oxidation is more stoichiometric than that by dry UV-oxidation, as expected [1]. The spectrum of the sample formed by UV oxidation in a flow of steam, as indicated by "wet + flow", shows a peak as narrow as a peak of thermally grown oxide and its peak position is extremely close to that of thermally grown oxide, suggesting that the stoichiometric oxide was formed by UV oxidation in a continuous steam flow. This sample was made in a flow of steam under UV irradiation so that the sample was always exposed to fresh steam, while the other samples were UV-oxidized in an enclosed chamber filled with O_2 or steam.

The high-frequency C-V characteristics of the wet UV-oxidized samples are shown in Fig. 2. The capacitances were measured by biasing the gate from -7 to 3 V and then from 3 to -7 V to check the hysteresis. The ideal C-V curve should show no hysteresis, as seen in the C-V curve of thermally grown oxide. The C-V curve of the sample with a steam flow shows an extremely small hysteresis and is much similar to that of thermally grown oxide than that of the sample without a steam flow.

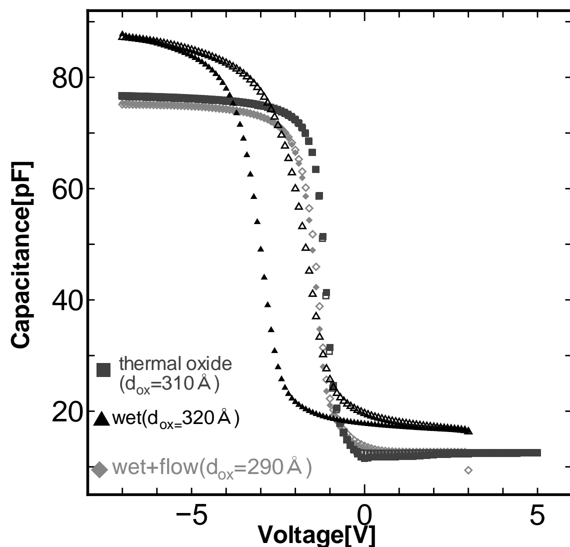

Fig. 2 High-frequency C-V characteristics of the wet UV-oxidized samples with and without a steam flow. The gate bias was ramped up from -7 to 3 V and then ramped down from 3 to -7 V to see the hysteresis. Open and closed symbols are for ramp-down and ramp-up gate bias, respectively. The thicknesses were measured with an ellipsometer.

Figure 3 shows the intereface state density profiles of the wet UV-oxidized samples with and without a steam flow. The interface state density at the midgap for wet UV-oxidized sample without a stem flow is 4 x 10^{11} $cm^{-2}eV^{-1}$ and is lower than that value 1 x 10^{12} $cm^{-2}eV^{-1}$ reported earlier [1]. The improvement is due to the increased bubbler's temperature, resulting in the increased water vapor pressure. The steam flow further deceases the midgap interface state density to 1 x 10^{11} $cm^{-2}eV^{-1}$. This value is compared with the values found in the literature [3]

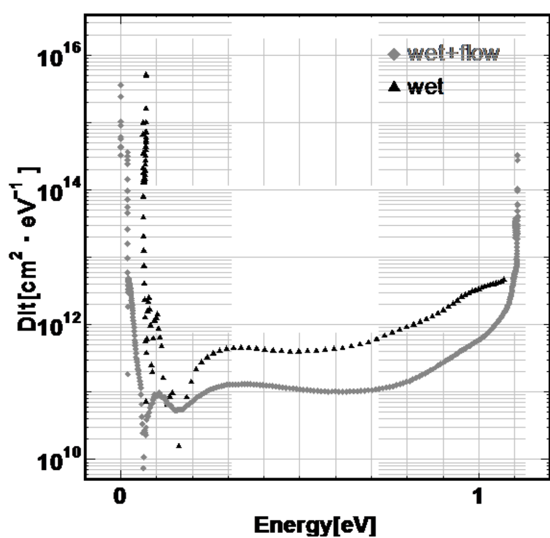

Fig. 3 Interface state density profiles of wet UV-oxidized samples with and without a steam flow. The interface state density was calculated as a function of the energy from 0 (the valence band edge) to 1.1 eV (the conduction band edge).

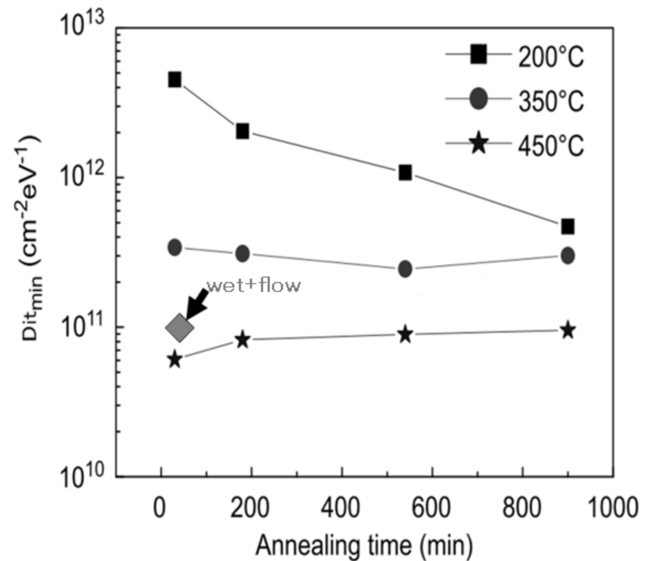

Fig. 3 The minimum values of the interface state density of the SiO_x films deposited at room temperature by ECR-PECVD. The MOS capacitor samples were annealed in a forming gas atmosphere at various temperatures for various periods of time.

in Fig. 4. In the reference, the SiO_x films were deposited at room temperature by ECR-PECVD, and then MOS capacitors were annealed at various temperatures and for various periods of time. The shortest annealing time was 30 min. The quasi-static C-V of the as-deposited film could not be measured because of large leakage current. Although the film was deposited at room temperature, annealing temperature of 450 ^oC was required to lower the interface state density to 10^{11} $cm^{-2}eV^{-1}$. In comparison to the ECR-CVD-deposited samples, our sample made at 200 ^oC by a simple process consisting of the vacuum evaporation of SiO nanopowder and post UV oxidation has a midgap interface state density as low as that of the ECR-CVD deposited sample post-annealed at 450 ^oC. To our knowledge, the midgap interstate density we obtained is the lowest ever reported for the MOS capacitors with the gate dielectric formed at 200 ^oC.

3. Conclusions

High-quality gate oxide has been formed at 200 ^oC by a rather simple process consisting of vacuum evaporation of SiO nanopowder and post UV oxidation. A midgap interface state density of 1 x 10^{11} $cm^{-2}eV^{-1}$ was achieved by making a continuous flow of steam during UV oxidation. The low-temperature process to form such high-quality gate oxide is a key technology in flexible electronics.

References

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