Fabrication of ZrSiO/Ge Gate Stacks with GeO₂ and ZrGeO Interlayers

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1. Introduction

Ge is of great interest as a candidate channel material for future CMOS devices due to its higher intrinsic carrier mobility. To realize Ge-CMOS technology, one of the most challenging issues is formation of a good high-k gate stack, and both thin EOT less than 1.0 nm and low Dₓ less than 1×10¹¹ cm⁻² eV⁻¹ are mandatory. Recent studies on high-k/Ge gate stacks have rapidly progressed. For an example, the gate stacks fabricated using an ECR plasma postoxidation through a thin Al₂O₃ showed a EOT of approximately 1.0 nm and a Dₓ of lower than 1×10¹¹ cm⁻² eV⁻¹ near the midgap.¹)

Our group has proposed a method for electrical passivation of a Ge surface by an ultrathin SiO₂/GeO₂ bilayer and achieved high-quality interface with a Dₓ of 1×10¹¹ cm⁻² eV⁻¹ near the midgap.² ³ By using this bilayer passivation (BLP), we fabricated n- and p-MOSFETs on Ge (100) substrates and demonstrated the high electron and hole mobilities of 1097 and 376 cm²V⁻¹s⁻¹, respectively.⁴ However, EOT of the SiO₂ gate stack used in the MOSFET fabrication was approximately 50 nm, while EOT of GeO₂ interlayer (IL) was less than 2 nm. In order to enhance the current drivability, EOT should be decreased.

In this study, we fabricated ZrSiO/Ge high-k gate stack with GeO₂ IL and ZrGeO IL. The structural and electrical properties of these gate stacks are presented.

2. Experimental Procedure and Structural Analysis

A p-type (100) Ge with a resistivity of 0.2 Ωcm was used. Fabrication process flow for high-k gate stack with GeO₂ IL is shown in Fig. 1. First, sacrificial oxidation was done at 450°C for 30 min by dry oxidation, followed by loading in a physical vapor deposition (PVD) chamber for BLP. After volatilization of GeO₂ by vacuum annealing, a 0.5 nm-thick SiO₂ was deposited on the Ge surface at 350°C using magnetron sputtering from a SiO₂ target without the addition of O₂. Then, postdeposition oxidation (PDO) was done at 450°C for 10 min in dry O₂. It was confirmed from XPS that a GeO₂ layer grows during PDO, as shown in Fig. 2. Furthermore, the cross sectional TEM analysis suggested that the GeO₂ thickness was 0.5 nm. On the sample with 0.5 nm-thick SiO₂/0.5 nm-GeO₂/Ge structure, 2 nm-thick Zr film was deposited using magnetron sputtering at room temperature (RT), followed by the deposition of 0.45 nm-thick SiO₂ with the addition of O₂. The XPS results of samples before and after the SiO₂/Zr depositions are shown in Fig. 3, indicating that the Si 2p core level of a sample with the SiO₂/Zr depositions shifted by 1.0 eV to lower binding energy relative to SiO₂. This implies that Zr reacts with SiO₂ during the sputter depositions, resulting in the formation of Zr silicate (ZrSiO).⁵ After the depositions, PDA was performed at 550°C for 30 min in N₂. Then, Al/TiN metal-gate process in Ref. 3 was done, which were the deposition of a TiN film, PMA at 450°C for 20 min, the evaporation of Al, the electrode patterning with an area of 2.25×10⁻² cm², and the contact annealing at 350°C for 10 min.

Fig. 1. Fabrication process flow of Ge-MOS capacitor with structure of ZrSiO/GeO₂-IL/Ge.

Fig. 2. Ge 3d XPS spectra for 0.5 nm-thick SiO₂ deposited sample. (a) and (b) are the results before and after PDO at 450°C for 10 min, respectively.

Fig. 3. Si 2p XPS spectra of samples (a) before and (b) after the SiO₂/Zr depositions. The spectrum (c) represents after PDA at 550°C for 30 min.
The fabrication of high-k gate stack with ZrGeO IL is simple. A 2 nm-thick Zr film was directly deposited on Ge surface at RT using sputtering. It was confirmed from TEM and EDX analyses that Zr reacts with Ge, resulting in the formation of Zr germanide (ZrGe) during the sputtering, as shown in Fig. 4. The TEM analysis showed the thickness of ZrGe layer was approximately 2 nm. Then, 0.7 nm-thick SiO\textsubscript{2} film was deposited with the addition of O\textsubscript{2} at RT, and PDA was done at 500°C for 30 min in N\textsubscript{2}. Finally, Al/TiN metal-gate process was performed.

3. Results and Discussion

Figure 5 (a) shows the C-V\textsubscript{G} characteristics for high-k gate stack with GeO\textsubscript{2} IL. The EOT, hysteresis (HT), flat band voltage (V\textsubscript{fb}), and leakage current density (J\textsubscript{leak}) at V\textsubscript{fb}-1 V are summarized in Table 1. The EOT of 1.6 nm is in good agreement with the estimation value (1.6 nm) using the permittivities and thicknesses of ZrSiO and GeO\textsubscript{2} layers (12 and 5.7, 4.0 and 0.5 nm). The J\textsubscript{leak} was 5×10\textsuperscript{-4} A/cm\textsuperscript{2}, which is 4 orders of magnitude lower than that of SiO\textsubscript{2} with the same EOT. The energy distribution of D\textsubscript{a} is plotted in Fig. 5(b), which was measured using DLTS. The D\textsubscript{a} distribution is similar to that of GeO\textsubscript{2}/Ge\textsuperscript{6} implying that GeO\textsubscript{2} played a role of IL. Thus, a capacitor with an EOT of 1.6 nm and a D\textsubscript{a} of 3×10\textsuperscript{11} cm\textsuperscript{-2}eV\textsuperscript{-1} near the midgap could be successfully fabricated. However, EOT is still thick to satisfy the requirement of high-k gate stack. We chose GeO\textsubscript{2} as an alternative high-k IL.

Figure 6 (a) show the C-V\textsubscript{G} characteristics for high-k gate stack with ZrGeO IL. The EOT, HT, V\textsubscript{fb}, and J\textsubscript{leak} at V\textsubscript{fb}-1 V are summarized in Table 1. An EOT of 0.99 nm could be achieved, which maybe originated from an increase in ZrSiO permittivity due to a decrease in Si content and higher permittivity of ZrGeO IL. The J\textsubscript{leak} was as low as 2×10\textsuperscript{-4} A/cm\textsuperscript{2} for an EOT of 0.99 nm, which is 4 orders of magnitude lower than that of SiO\textsubscript{2}. Thus, the high-k gate stack fabricated in this study is a candidate as a gate stack towards embodying EOT less than 1.0 nm. Furthermore, the well-behaved C-V\textsubscript{G} curve means that ZrGeO played a role of IL. The energy distribution of D\textsubscript{a} is plotted in Fig. 6(b). The D\textsubscript{a} near the midgap is higher than that with GeO\textsubscript{2}, but the D\textsubscript{a} near the valence band is comparable. Considering an extremely low EOT of around 0.5 nm needed for future CMOS, IL should be composed by high-k materials. Although the D\textsubscript{a} is still high, further decrease in D\textsubscript{a} would be possible by combining the present gate stack fabrication technique with the strict surface cleaning technique.

4. Conclusion

We fabricated ZrSiO/Ge gate stacks with two kinds of IL, which were ultrathin GeO\textsubscript{2} and ZrGeO. The MOS capacitor with GeO\textsubscript{2}-IL showed EOT=1.6 nm and D\textsubscript{a}=3.5×10\textsuperscript{11} cm\textsuperscript{-2}eV\textsuperscript{-1} near the midgap. The MOS capacitor with ZrGeO IL showed EOT of 0.99 nm and D\textsubscript{a}=9.5×10\textsuperscript{11} cm\textsuperscript{-2}eV\textsuperscript{-1}. The J\textsubscript{leak} for both capacitors were 4 orders of magnitude lower than that of SiO\textsubscript{2} with the same EOT.

References


Table 1. EOT and HT, V\textsubscript{fb}, J\textsubscript{leak} obtained from C-V\textsubscript{G} and J-V\textsubscript{G} characteristics.

<table>
<thead>
<tr>
<th>IL</th>
<th>EOT [nm]</th>
<th>HT [mV]</th>
<th>V\textsubscript{fb} [V]</th>
<th>J\textsubscript{leak} [A/cm\textsuperscript{2}]@V\textsubscript{fb}=-1V</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)GeO\textsubscript{2}-IL</td>
<td>1.58</td>
<td>133</td>
<td>0.13</td>
<td>4.7×10\textsuperscript{-4}</td>
</tr>
<tr>
<td>(b)ZrGeO \textsubscript{x}-IL</td>
<td>0.99</td>
<td>85</td>
<td>0.66</td>
<td>2.2×10\textsuperscript{-4}</td>
</tr>
</tbody>
</table>

Fig.4 TEM and EDX results for the sample deposited with Zr on Ge.

Fig.5 (a) C-V\textsubscript{G} characteristic and (b) the energy distribution of D\textsubscript{a} for high-k gate stack with GeO\textsubscript{2} IL.

Fig.6 (a) C-V\textsubscript{G} characteristics and (b) the energy distribution of D\textsubscript{a} for high-k gate stack with ZrGeO IL.