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Fabrication of ZrSiO/Ge Gate Stacks with GeO_2 and ZrGeO Interlayers

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1. Introduction

Ge is of great interest as a candidate channel material for future CMOS devices due to its higher intrinsic carrier mobility. To realize Ge-CMOS technology, one of the most challenging issues is formation of a good high-*k* gate stack, and both thin EOT less than 1.0 nm and low D_{it} less than 1×10^{11} cm^{-2} eV^{-1} are mandatory. Recent studies on high-*k*/Ge gate stacks have rapidly progressed. For an example, the gate stacks fabricated using an ECR plasma postoxidation through a thin Al_2O_3 showed a EOT of approximately 1.0 nm and a D_{it} of lower than 1×10^{11} $cm^{-2}eV^{-1}$ near the midgap.[1)]

Our group has proposed a method for electrical passivation of a Ge surface by an ultrathin SiO_2/GeO_2 bilayer and achieved high-quality interface with a D_{it} of 1×10^{11} $cm^{-2}eV^{-1}$ near the midgap.[2, 3)] By using this bilayer passivation (BLP), we fabricated n- and p-MOSFETs on Ge (100) substrates and demonstrated the high electron and hole mobilities of 1097 and 376 $cm^2V^{-1}s^{-1}$, respectively.[4)] However, EOT of the SiO_2 gate stack used in the MOSFET fabrication was approximately 50 nm, although EOT of GeO_2 interlayer (IL) was less than 2 nm. In order to enhance the current drivability, EOT should be decreased.

In this study, we fabricated ZrSiO/Ge high-*k* gate stack with GeO_2 IL and ZrGeO IL. The structural and electrical properties of these gate stacks are presented.

2. Experimental Procedure and Structural Analysis

A p-type (100) Ge with a resistivity of 0.2 Ωcm was used. Fabrication process flow for high-*k* gate stack with GeO_2 IL is shown in Fig. 1. First, sacrificial oxidation was done at 450°C for 30 min by dry oxidation, followed by loading in a physical vapor deposition (PVD) camber for BLP. After volatilization of GeO_2 by vacuum annealing, a 0.5 nm-thick SiO_2 was deposited on the Ge surface at 350°C using magnetron sputtering from a SiO_2 target

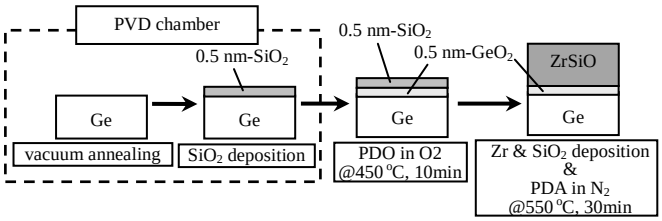

Fig. 1. Fabrication process flow of Ge-MOS capacitor with structure of ZrSiO/GeO_2-IL/Ge.

without the addition of O_2. Then, postdeposition oxidation (PDO) was done at 450°C for 10 min in dry O_2. It was confirmed from XPS that a GeO_2 layer grows during PDO, as shown in Fig. 2. Furthermore, the cross sectional TEM analysis suggested that the GeO_2 thickness was 0.5 nm. On the sample with 0.5 nm-thick SiO_2/0.5 nm-GeO_2/Ge structure, 2 nm-thick Zr film was deposited using magnetron sputtering at room temperature (RT), followed by the deposition of 0.45 nm-thick SiO_2 with the addition of O_2. The XPS results of samples before and after the SiO_2/Zr depositions are shown in Fig. 3, indicating that the Si 2*p* core level of a sample with the SiO_2/Zr depositions shifted by 1.0 eV to lower binding energy relative to SiO_2. This implies that Zr reacts with SiO_2 during the sputter depositions, resulting in the formation of Zr silicate (ZrSiO).[5)] After the depositions, PDA was performed at 550°C for 30 min in N_2. Then, Al/TiN metal-gate process in Ref. 3 was done, which were the deposition of a TiN film, PMA at 450°C for 20 min, the evaporation of Al, the electrode patterning with an area of 2.25×10^{-4} cm^2, and the contact annealing at 350°C for 10 min.

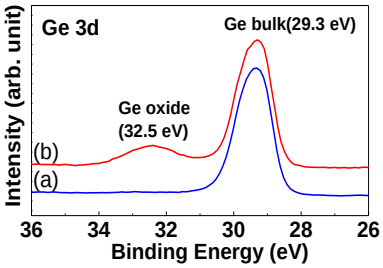

Fig. 2. Ge 3*d* XPS spectra for 0.5 nm-thick SiO_2 deposited sample. (a) and (b) are the results before and after PDO at 450°C for 10 min, respectively.

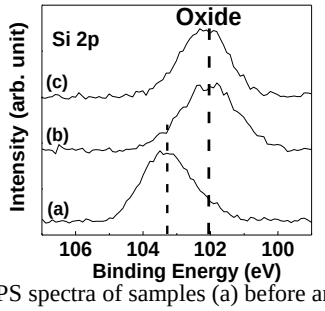

Fig. 3. Si 2*p* XPS spectra of samples (a) before and (b) after the SiO_2/Zr depositions. The spectrum (c) represents after PDA at 550°C for 30 min.

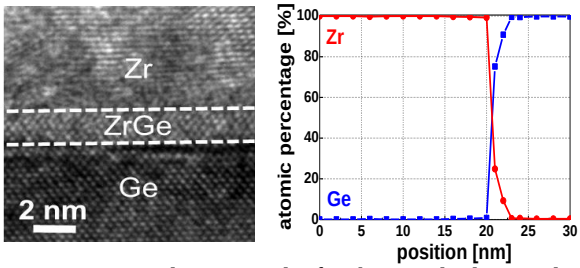

Fig.4 TEM and EDX results for the sample deposited with Zr on Ge.

The fabrication of high-*k* gate stack with ZrGeO IL is simple. A 2 nm-thick Zr film was directly deposited on Ge surface at RT using sputtering. It was confirmed from TEM and EDX analyses that Zr reacts with Ge, resulting in the formation of Zr germanide (ZrGe) during the sputtering, as shown in Fig. 4. The TEM analysis showed the thickness of ZrGe layer was approximately 2 nm. Then, 0.7 nm-thick SiO_2 film was deposited with the addition of O_2 at RT, and PDA was done at 500°C for 30 min in N_2. Finally, Al/TiN metal-gate process was performed.

3. Results and Discussion

Figure 5 (a) shows the C-V_G characteristics for high-*k* gate stack with GeO_2 IL. The EOT, hysteresis (HT), flat band voltage (V_{fb}), and leakage current density (J_{leak}) at V_{fb}-1 V are summarized in Table 1. The EOT of 1.6 nm is in good agreement with the estimation value (1.6 nm) using the permittivities and thicknesses of ZrSiO and GeO_2 layers (12 and 5.7, 4.0 and 0.5 nm). The J_{leak} was 5×10^{-4} Acm^{-2}, which is 4 orders of magnitude lower than that of SiO_2 with the same EOT. The energy distribution of D_{it} is plotted in Fig. 5(b), which was measured using DLTS. The D_{it} distribution is similar to that of GeO_2/Ge,[6] implying that GeO_2 played a role of IL. Thus, a capacitor with an EOT of 1.6 nm and a D_{it} of 3×10^{11} cm^{-2}eV^{-1} near the midgap could be successfully fabricated. However, EOT is still thick to satisfy the requirement of high-*k* gate stack. We chose ZrGeO as an alternative high-*k* IL.

Figure 6 (a) show the C-V_G characteristics for high-*k* gate stack with ZrGeO IL. The EOT, HT, V_{fb}, and J_{leak} at V_{fb}-1 V are summarized in Table 1. An EOT of 0.99 nm could be achieved, which maybe originated from an increase in ZrSiO permittivity due to a decrease in Si content and higher permittivity of ZrGeO IL. The J_{leak} was as low as 2×10^{-1} Acm^{-2} for an EOT of 0.99 nm, which is 4 orders of magnitude lower than that of SiO_2. Thus, the high-*k* gate stack fabricated in this study is a candidate as a gate stack towards embodying EOT less than 1.0 nm. Furthermore, the well-behaved C-V_G curve means that ZrGeO played a role of IL. The energy distribution of D_{it} is plotted in Fig. 6(b). The D_{it} near the midgap is higher than that with GeO_2, but the D_{it} near the valence band is comparable. Considering an extremely low EOT of around 0.5 nm needed for future CMOS, IL should be composed by high-*k* materials. Although the D_{it} is still high, further decrease in D_{it} would be possible by combining the present gate stack fabrication technique with the strict surface cleaning technique.

4. Conclusion

We fabricated ZrSiO/Ge gate stacks with two kinds of IL, which were ultrathin GeO_2 and ZrGeO. The MOS capacitor with GeO_2-IL showed EOT=1.6 nm and D_{it}= 3.3×10^{11} cm^{-2}eV^{-1} near the midgap. The MOS capacitor with ZrGeO IL showed EOT of 0.99 nm and D_{it}=9.5×10^{11} cm^{-2}eV^{-1}. The J_{leak} for both capacitors were 4 orders of magnitude lower than that of SiO_2 with the same EOT.

References

[1]R. Zhang et al., IEEE Trans. Electron Devices **59** (2012) 335.
[2]K. Hirayama et al., Jpn. J. Appl. Phys. **50** (2011) 04DA10.
[3]H. Nakashima et al., Appl. Phys. Lett. **98** (2011) 252102.
[4]K. Yamamoto et al., Appl. Phys. Express **4** (2011) 051301.
[5]H. Watanabe, Appl. Phys. Lett. **81** (2002) 4221.
[6]H. Matsubara et al., Appl. Phys. Lett. **93** (2008) 032104.

Table. 1. EOT and HT, V_{fb}, J_{leak} obtained from C-V_G and J-V_G characteristics.

	(a)GeO_2-IL	(b)$ZrGeO_x$-IL
EOT[nm]	1.58	0.99
HT[mV]	133	85
V_{fb}[V]	0.13	0.06
J_{leak}[A/cm^2]@V_{fb}-1V	4.7×10^{-4}	2.2×10^{-1}

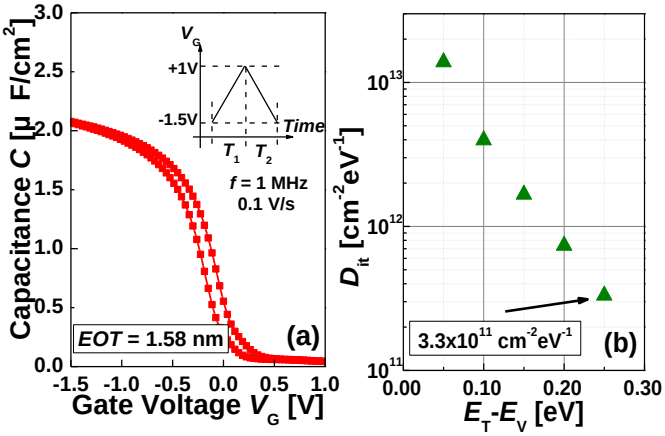

Fig.5 (a) C-V_G characteristic and (b) the energy distribution of D_{it} for high-*k* gate stack with GeO_2 IL.

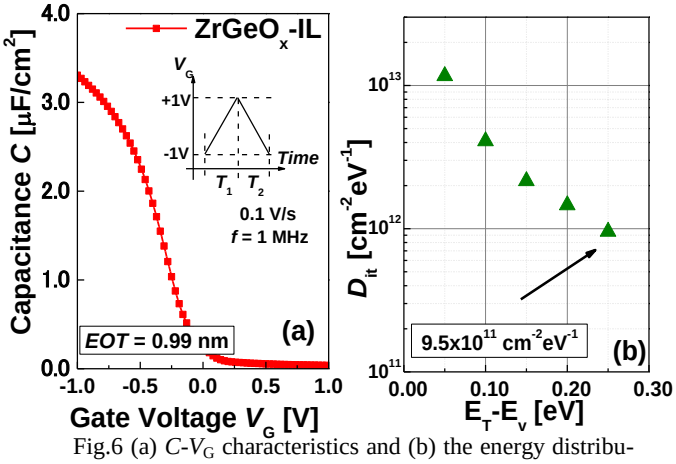

Fig.6 (a) C-V_G characteristics and (b) the energy distribution of D_{it} for high-*k* gate stack with ZrGeO IL.