Impacts of interfacial insulator on poly-crystalline germanium growth in low temperature processing

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1. Introduction

Germanium (Ge) is considered to be promising materials to realize not only for high mobility more Moore technology but also for more than Moore application such as 3D-LSI [1] or "channel-last devices" such as BiCS Flash Memory [2], because of its higher carrier mobility as well as the low processing temperature. In fact, solid phase crystallization (SPC) of amorphous Ge (*a*-Ge) has been demonstrated at low temperature [3]. In this study, we focus on effects of the interfacial insulator on Ge crystallization and on electrical properties of polycrystalline Ge (poly-Ge) TFTs.

2. Fabrication of poly-Ge TFTs

We prepared Y_2O_3 , Al_2O_3 or GeO_2 by rf-sputtering on SiO₂ thermally grown on n⁺-Si(100) substrate, followed by annealing in N₂+O₂ ambient for 30 sec at 600°C. 20-nm thick *a*-Ge was evaporated in UHV (**Fig. 1(a)-(b)**). Subsequently, 80-nm SiO₂ was deposited as the capping layers, which suppressed the roughening of poly-Ge surface during SPC. SPC was carried out by the two-step annealing [3]. After removing the capping layer, several length Ge islands were defined by wet etching, and Al was deposited and patterned for source/drain for selected Ge islands. Al was also deposited on the backside of Si wafer as the back gate electrode. Raman spectroscopy measurement was performed for analyzing the crystallized films, and I-V characteristics in poly-Ge TFTs were measured (**Fig. 1(c**)).

3. Result and Discussion

It is reported that GeO_2/Ge intrinsically has as a good interface as SiO_2/Si [5, 6], and that rare-earth materials are very intimate with Ge [7]. 20-nm Ge deposited on GeO₂, however, disappeared during SPC by the reaction of Ge with GeO₂ [4]. Good interface of GeO₂ on Ge wafer is not applicable for poly-Ge growth on GeO₂.

Fig. 2 shows electrical properties of poly-Ge TFTs fabricated on three kinds of insulators. The clear difference in (a) I_d - V_g characteristics of poly-Ge TFTs indicates that the selection of interfacial insulator is critically important for achieving better TFT in terms of both on/off ratio and on-current. The best FET result in this study was observed in the case fabricated on SiO₂ as shown in **Fig. 2(b)**. Although the highest field effect



Fig. 1. Schematic of samples. Amorphous Ge films were deposited on (a) SiO₂, (b) Y_2O_3 , Al₂O₃ or GeO₂, deposited on SiO₂ by rf-sputtering,, and then (c)poly-Ge TFT were fabricated.



Fig. 2. (a) Transfer characteristics of poly-Ge TFT fabricated on various insulators. On SiO₂, the highest field effect mobility was 40 cm²/Vs. (b) Output characteristic of poly-Ge TFT fabricated on SiO₂.

mobility obtained so far in our study is about 40 cm²/Vsec which is still lower than the best reported value in poly-Ge TFT [8], it is already higher than poly-Si TFT fabricated by SPC [9] and can be further improved.

To investigate the origin of these differences in electrical properties, we compared the resistivity and the crystallinity of poly-Ge films on three kinds of insulators, where the latter was evaluated by Raman spectroscopy. As shown in Fig. 3, the FWHM of Ge peak in Raman spectra on Y_2O_3 is larger than that on SiO₂ or on Al₂O₃. It indicates that poly-Ge on Y_2O_3 has smaller crystallites compared with those on SiO₂ or Al₂O₃, by assuming that the FWHM is attributable to a relaxation of the q-selection rule with decreasing grain size and the disappearance of long range order [10]. Thus, the crystallinity of poly-Ge grown on Y2O3 is poor, resulting in the lower on-current of poly-Ge TFT because of the existence of more grain boundaries which can be the potential barriers for carrier transport. On the other hand, there are no differences of the resistivity and crystallinity in poly-Ge films between on SiO₂ and on Al₂O₃, while the on/off ratio is clearly larger in poly-Ge on SiO₂. It is inferred that there might be more defects at the poly-Ge/Al₂O₃ interface than those at poly-Ge/SiO₂, though the bulk Ge properties are roughly the same. This is quite consistent with the subthreshold characteristics difference in TFT between on SiO₂ and Al₂O₃.

To clarify the reason for the crystallinity degradation of poly-Ge on Y_2O_3 , we evaluated the incubation time of SPC on three kinds of insulators. After annealing a-Ge/insulator/Si (as shown in Fig. 1(a) and (b)) at 500° C in N₂ ambient for 5~15min, the crystallinity (X_c) was evaluated by using the following equation:

 $X_c = (S_c+S_{\mu})/(S_c+S_{\mu}+S_a)$, where S_c , S_{μ} and S_a are the integrated Raman peak intensities corresponding to amorphous Ge, microcrystalline Ge (µ-Ge) and crystalline Ge (c-Ge), respectively, which are derived from the three-peak fitting method with weighted gaussian function [11]. Fig. 4 shows crystallinity of poly-Ge on three kinds of insulators as a function of annealing time. It is clearly observed that the nucleation of *a*-Ge starts in the shorter annealing time on Y_2O_3 than on SiO₂ and on Al₂O₃. It indicates that the nucleation of a-Ge can occur more easily on Y_2O_3 , and that the size of crystallites should be smaller. It is likely that the nucleation from a-Ge occurs more easily on the insulator



Fig. 3. Values of the resistivity and the FWHM in Raman spectra of poly-Ge fabricated on various insulators.



Fig. 4. (a) Time dependence of the crystallinity of poly-Ge fabricated on various insulators, calculated from Raman spectra by using (b) 3-peak fitting method.

which shows good electrical properties on single crystalline Ge. It is inferred that the YGeO_x formation at Ge/Y₂O₃ interface may promote the migration of Ge atoms near the interface and accelerate the nucleation of a-Ge on Y_2O_3 easier than on SiO₂ and on Al₂O₃. Fig. 5 shows a schematic view of the crystallization process about why Y₂O₃ surface can drive the Ge crystallization. Through the mixing process of Ge with Y_2O_3 , the Ge crystallization energy barrier may be lowered thanks to the easy bond breaking in a-Ge and the critical nucleation radius is likely to be reduced, though the further investigation is obviously needed to clarify the microscopic origin.



Fig. 5. Schematic images of the interface-accelerated nucleation. (a) Ge bonds are easily broken on Y_2O_3 . (b) The energy barrier against Ge crystallization is lowered by the interface energy reduction due to the mixing.

4. Conclusions

We investigated poly-Ge TFTs fabricated on various insulators and demonstrated the importance of the interfacial insulator selection for making the best of Ge advantages in terms of the low temperature process. It is concluded that the insulator which is intimate with Ge substrate such as GeO_2 or Y_2O_3 , is not adequate for fabricating high performance Ge TFT.

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