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Interface Reaction Control by Gate Metal Selection for Improving Thermal Stability of La_2O_3-gated InGaAs MOS Capacitors

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1. Introduction

III-V material and in particular InGaAs are recognized as one of the leading candidates to replace Si as *n*-channel material in metal-oxide-semiconductor field effect transistors (MOSFETs) because of their higher injection velocity [1]. Recently high performance InGaAs MOFETs have been demonstrated, with most of the studies focusing on Al_2O_3 or HfO_2 as gate dielectric. Although significant progress has been made in improving dielectric/InGaAs interface, the best of these results have been reported for Al_2O_3/InGaAs interfaces. Thus scaling of InGaAs gate stacks has been very limited due to low dielectric constant (k ~ 9) of Al_2O_3 and its relatively small thermal processing window (< 400 ^oC). HfO_2 (only)-gated devices on the other hand, still exhibit large midgap interface state density (D_{it}) which degrades their device performance [2].

La_2O_3 (k ~ 24) can intermix with the substrate through the formation of Ga-O-La and In-O-La bonds (fig. 2 (a) to (c), fig. 3 (b)). Similar bonding patterns for La_2O_3 can be observed on Si-sub (La-silicate) and Ge-sub (La-germanate), which can significantly improve interface quality [3]. This is in contrast to HfO_2 which promotes the formation of Ga- and As-suboxides at HfO_2/InGaAs interface (fig. 2 (a) to (c), fig. 3 (a)). These suboxides are regarded as the main reason for increased D_{it} value in HfO_2 gate stacks [4].

In this study, the effect of gate metal on La_2O_3/$In_{0.53}Ga_{0.47}As$ interface quality is experimentally presented. It is shown for the first time that suppressing oxygen supply by employing Metal Inserted Poly-silicon (MIPS) stack, leads to significant improvement in C-V characteristics and thermal stability of La_2O_3/$In_{0.53}Ga_{0.47}As$ interface.

2. Experimental details

Capacitors were fabricated on S-doped *n*-$In_{0.53}Ga_{0.47}As$ (dopant: 2×10^{16} cm^{-3}) epiaxially grown on InP substrate. Substrates were degreased by acetone and ethanol and treated with concentrated HF and $(NH_4)_2S$ at room temperature for oxide removal and surface passivation. La_2O_3 film was deposited by e-beam evaporation and W gate electrode was in-situ deposited by RF magnetron sputtering. TiN and Si were subsequently deposited by RF sputtering to fabricate MIPS gate stacks. Post-metallization anneals (PMA) were carried out in forming gas (N_2:H_2= 97:3%) ambient for 5 min.

3. Results and discussion

The schematic in fig. 4 illustrates the effect of gate metal selection on controlling the amount of oxygen diffusion into gate stack. Fig. 5(a)- and (b)-bottom shows the C-V characteristics for capacitors with and without TiN capping layer. A qualitative comparison of these C-V curves already points to an improved interface property of capacitor with TiN/W gate electrode. For the capacitor with TiN/W -gated MOSCAPs, the capacitance in depletion reaches its ideal value of 0.07 μF/cm^2 and the upturn of capacitance in negative bias is suppressed for high frequencies. This indicates lower midgap interface state density and a sharper band-bending [5]. Also, the conductance [fig. 5(b)-up] is decreasing at increasing voltage and much lower at negative voltage compared to W-gated MOSCAP [fig. 5(a)-up]. This shows a smaller contribution from gate leakage current [6].The effect of annealing temperature on capacitance equivalent thickness (CET) growth for both gate structures is shown in fig. (6). Higher temperature tolerance of TiN/W-gated MOSCAPs could be due to suppressed interface reaction caused by oxygen-blocking effect of TiN capping layer. The added effect of oxygen barrier was investigated through MIPS structure [4], fabricated according to the flow shown in Fig. 7. The Si layer at the top of gate stack blocks the diffusion of oxygen even at higher annealing temperatures. Fig. 8 shows well behaved C-V curves for MIPS-stacked structure after annealing at 500 ^oC and a subsequent low temperature anneal at 320 ^oC after Si removal. Gate leakage current of three gate stacks with almost same CET is presented as a function of annealing temperature in Fig. 9. MIPS-stacked MOSCAPs have two orders of magnitude smaller leakage current density at higher annealing temperature.

4. Conclusion

It was shown that gate metal selection is a key factor in controlling La_2O_3/InGaAs interface reaction. Metal inserted poly-Si structure was found to be an effective structure for oxygen diffusion control and scalability potential.

Acknowledgements

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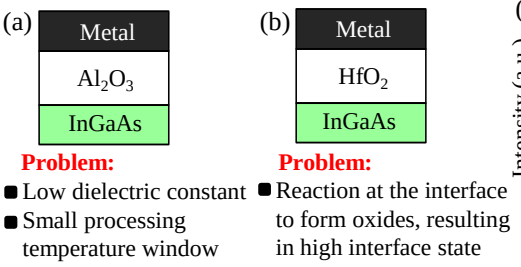


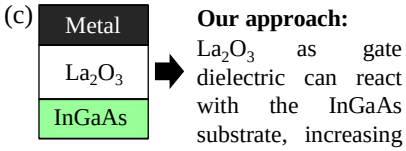
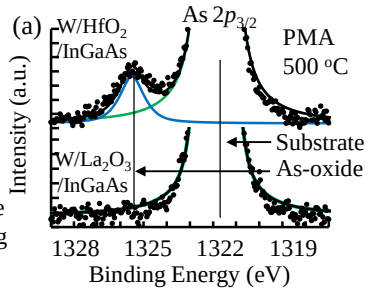
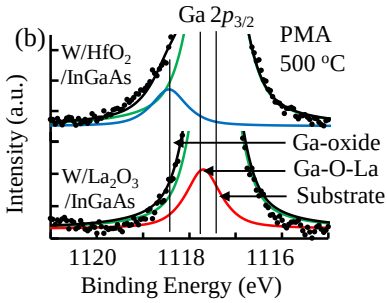


Fig. 1 Illustration of common dielectric/InGaAs interface issues.





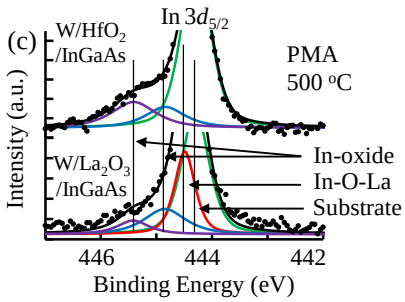


Fig. 2 XPS spectra of (a) As 2*p* (b) Ga 2*p* and (c) In 3*d* for W/HfO_2 (10 nm)/InGaAs and W/La_2O_3 (10 nm)/InGaAs.

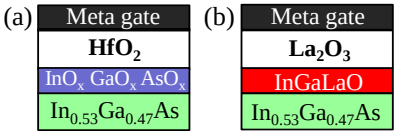


Fig. 3 Illustration of difference in La_2O_3/InGaAs and HfO_2/InGaAs interface reaction, triggered by oxygen diffusion..

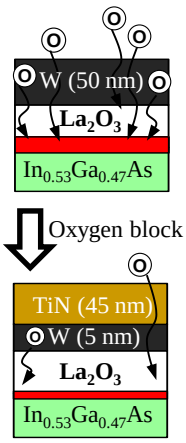


Fig. 4 Illustration of suppressing oxygen diffusion by using TiN/W gate metal.

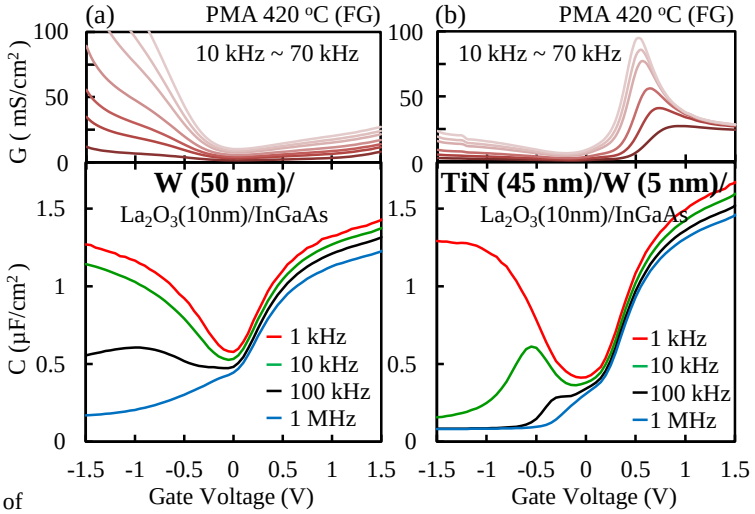


Fig. 5 Measured conductance (up) and C-V curves (bottom) of (a) W/La_2O_3(10nm)/InGaAs and (b) TiN/W/La_2O_3(10nm)/InGaAs capacitors as function of gate voltage after PMA in FG at 420 °C.

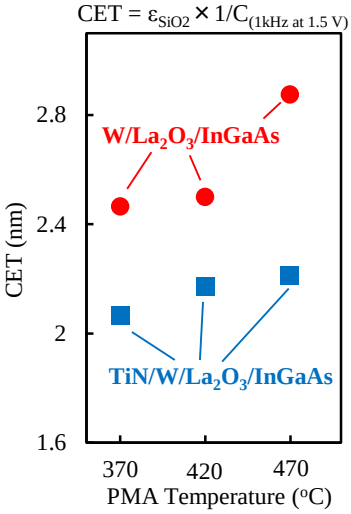


Fig. 6 Capacitance equivalent thickness of two gate stacks vs PMA temperature in FG.

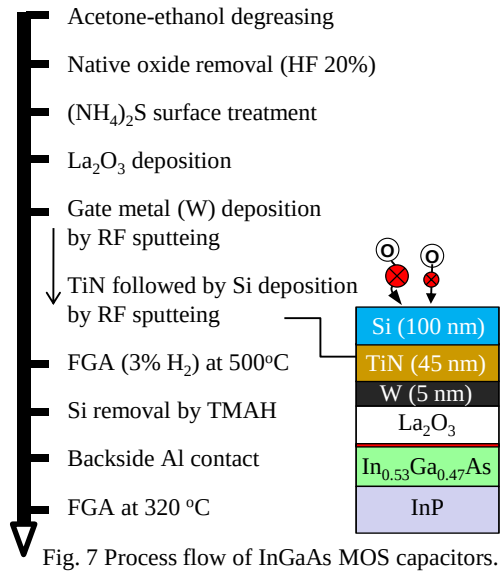


Fig. 7 Process flow of InGaAs MOS capacitors.

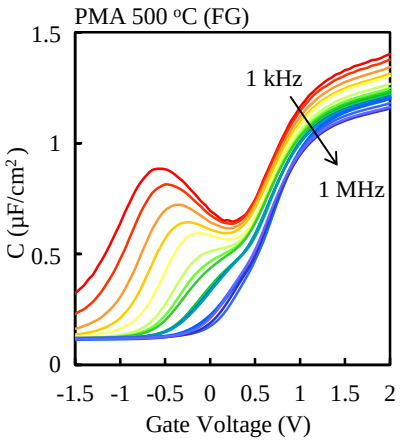


Fig. 8 C-V curves of MIPS structured (Si/TiN/W/La_2O_3(10nm)/InGaAs capacitor after FG annealing at 500 °C and Si removal.

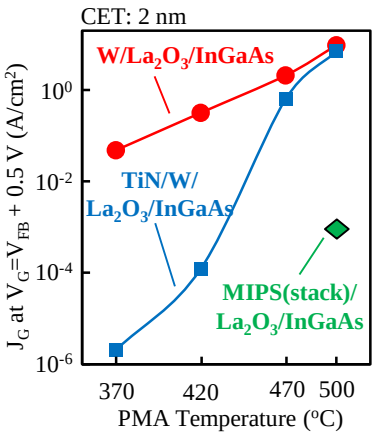


Fig. 9 Gate leakage current of three gate stacks at V_G=V_{FB} + 0.5 V as a function of PMA temperature.