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Ultrathin PVP Formation Utilizing Evaporation Method to Improve Pentacene/HfO_2 Interface Characteristics

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1. Introduction

Operating voltages required to achieve high hole mobility (μ) in pentacene based organic field-effect-transistors (OFETs) are generally higher than 20 V. Therefore, high-k gate insulators have been investigated in the pentacene based OFETs. However, inorganic high-k gate insulator usually does not provide good interface characteristics with organic channel materials. *Shin* et al. reported that poly(4-viniyl phenol) (PVP) interfacial layer to improve the pentacene/HfLaO interface characteristics [1]. However, the minimum thickness of PVP layer was 8 nm because it was formed by spin coating method. In this paper, we investigated ultrathin PVP layer formation, such as 3-10 nm, utilizing evaporation method for the first time to improve the pentacene/HfO_2 interface characteristics.

2. Experimental Procedure

Figure 1 shows the schematic sample structures fabricated in this study. Bottom gate type pentacene based OFETs were fabricated on n^+-Si(100) substrates with a top-contact bottom-gate device geometry [2]. n-Si(100) substrates were also used for some of the samples. Firstly, n^+-Si(100) substrates were chemically cleaned followed by the formation of chemical oxide layers, and the thickness of chemical oxide (C'O) layer is 0.7 nm. Then, HfO_2 thin films (5 nm) were deposited on the substrates by electron cyclotron resonance (ECR) plasma sputtering at room temperature (RT), and the pressure in the chamber during the deposition was 0.19 Pa (Ar/O_2 flow rate: 23/4.6 sccm). For comparison, SiO_2 (10 nm) layers were grown on n^+-Si(100) substrates by wet thermal oxidation at 850°C. After the fabrication of gate insulators, 3-10 nm-thick PVP layers (from Aldrich without any purification) were deposited on gate insulators by thermal evaporation at RT-150°C. Then, 20 nm-thick pentacene films were in-situ deposited (0.01 nm/s) on PVP interfacial layers at RT-70°C. The back pressure in the chamber was $2x10^{-6}$ Torr. Finally, Au and Al electrodes were evaporated. The channel width (W) and length (L) of the OFETs were 500 and 50 μm, respectively.

3. Results and Discussion

Figure 2 shows deposition temperature dependence on the surface RMS roughness of 3-10 nm-thick PVP formed on SiO_2/n-Si(100). The surface roughness was decreased with increasing the deposition temperature to 100°C especially for 5 nm-thick PVP (rms: 0.11 nm). On the other hand, the surface became rough when the deposition temperature was 150°C. Figure 3(a) shows C-V characteristics of Al/PVP/SiO_2/n-Si(100) diodes. PVP was deposited at 100°C. Excellent C-V characteristics were obtained, and the accumulation capacitance was decreased with the PVP thickness. The thickness and uniformity of the PVP layer was confirmed by cross-sectional TEM image as shown in Fig. 3(b). Figure 4 shows I_D-V_G and gate leakage current of pentacene based OFET with PVP/SiO_2 gate insulator. Pentacene was deposited at RT. Excellent device characteristics were confirmed such as I_{on}/I_{off} of $1.2x10^5$, subthreshold swing (SS) of 0.44 V/dec., and μ of 0.23 cm^2/Vs.

Next, the effect of PVP interfacial layer for pentacene based OFETs with HfO_2 gate insulator was investigated. Figure 5 shows deposition temperature dependence on the surface RMS roughness of 5 nm-thick PVP formed on HfO_2/n^+-Si(100). The surface rms roughness of 0.11 nm was obtained for the PVP films deposited at 50-100°C. Figure 6 shows C-V characteristics of MIM diodes with HfO_2 and PVP/HfO_2 gate insulators. The PVP layer was deposited at 50°C. No frequency dispersion was observed, and thin capacitance equivalent thickness (CET) of 7.7 nm was obtained for PVP/HfO_2 gate insulator. Figure 7 shows I_D-V_G characteristics of pentacene based OFET with PVP/SiO_2 gate insulator. The deposition temperature of pentacene was RT. The device characteristics were found to be improved for the OFET with PVP/HfO_2 gate insulator such as SS of 0.41 V/dec. and μ of 0.32 cm^2/Vs. Not only the interface characteristics but the grain growth of pentacene was enhanced by PVP as shown in Fig. 8.

4. Conclusions

Ultrathin (3-10 nm) PVP layers were formed by evaporation method for the first time. Excellent device characteristics were realized utilizing PVP interface layer.

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References

[1] W.C. Shin et al., IEEE EDL, **31** (2010) 1308.
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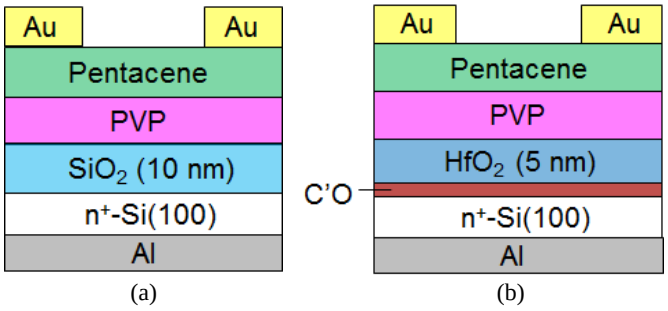

Fig. 1. Schematics of bottom gate type pentacene based OFETs fabricated in this study. (a) PVP/SiO_2 and (b) PVP/HfO_2 gate insulator.

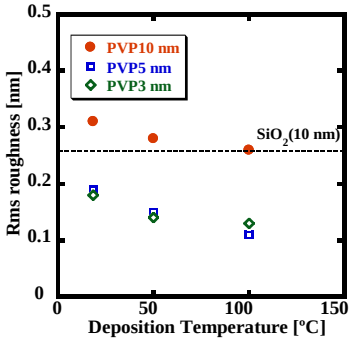

Fig. 2. Deposition temperature dependence on surface rms roughness of PVP layers deposited on SiO_2/n-Si(100).

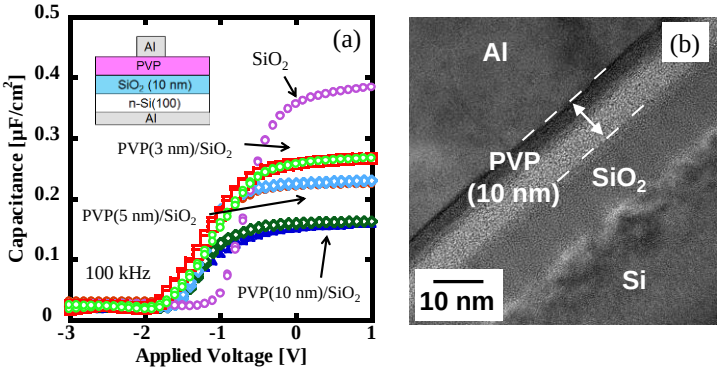

Fig. 3. (a) C-V and (b) cross-sectional TEM image of Al/PVP/SiO_2/n-Si(100) diodes.

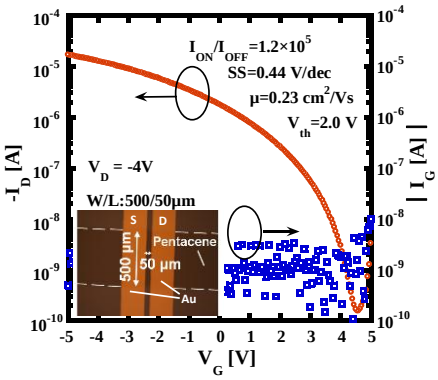

Fig. 4. I_D-V_G and gate leakage current of pentacene based OFETs with PVP/SiO_2 gate insulator. The plane view of the fabricated device is indicated as an inset.

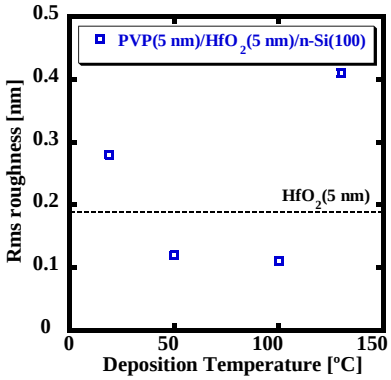

Fig. 5. Deposition temperature dependence on surface rms roughness of PVP layers deposited on HfO_2/n-Si(100).

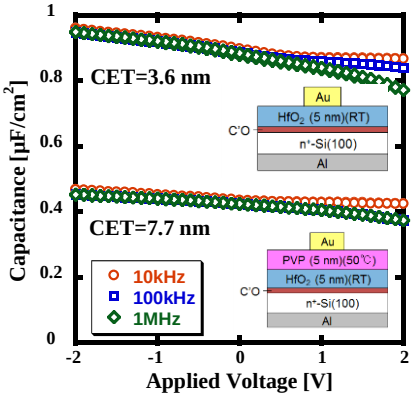

Fig. 6. C-V characteristics of Au/HfO_2/n^+-Si(100) and Au/PVP/HfO_2/n^+-Si(100) diodes.

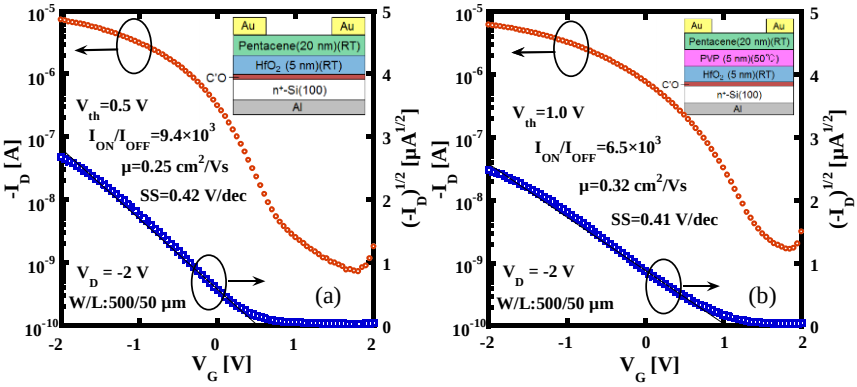

Fig. 7. I_D-V_G characteristics of pentacene based OFETs with (a) HfO_2 (b) PVP/HfO_2 gate insulator.

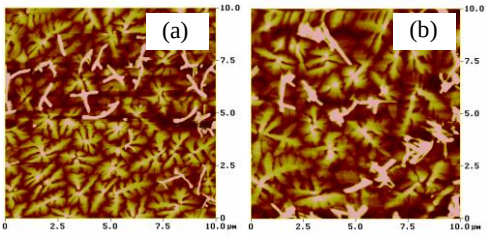

Fig. 8. AFM images of pentacene deposited on (a) HfO_2/n^+-Si(100) and (b) PVP/HfO_2/n^+-Si(100).