Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp436-437

Comparison of Electro-Optic Effect based Graphene Transistors

Gaurav Gupta, Mansoor Bin Abdul Jalil and Gengchiau Liang†
Department of Electrical and Computer Engineering, National University of Singapore, Singapore
†Phone: +65-6516-2898 E-mail: elelg@nus.edu.sg

1. Introduction

Low sub-threshold slope (SS) is required for future high-speed and low-power consumption switch which can toggle between high switch-on current (I_{ON}) for faster charging of load capacitors, and low switch-off current (I_{OFF}) for lower static dissipation for small gate voltage swing. The traditional MOSFET architecture, however, limits SS to 60mV/dec. at 300K. Although other Si-MOS architectures like feedback MOSFET, NEMFET and TFET have been researched, their trade-offs among performance metrics [1] have motivated research on graphene transistors because of latter's superior mobility and longer mean free path [2]. Unfortunately, it has been known that lack of bandgap in graphene has demeaned its prospects as FET for logic devices. Therefore, non-conventional transistors, exploiting new physical phenomenon like pseudo-spin, Klein paradox and electro-optic effect [3], have been proposed to circumvent these limitations. Recently, the experimental proof of electro-optic mechanism [4] in graphene has resulted in proposal for graphene electro-optic transistors (GEOT) [5][6].

In this work, we present a computational comparison of device performance for two proposed GEOT devices, namely design A [6] and design B [7], as shown in Fig. 1. These two different designs have been evaluated for device geometry, temperature and voltage conditions. We observed that although the device characteristics and performance of these two designs are comparable, with consideration of some specific advantages and disadvantages of each design w.r.t SS, I_{ON}, I_{ON}/I_{OFF} and device fabrication, design B is found to have overall better performance.

2. Theory and Methodology

As shown in Fig. 1, the device structure and the top view of two GEOT devices are presented for ideal (pure 2D) undoped channel with two gates (V_{G1} and V_{G2}), with abrupt junction and no edge effects. For ballistic transport, the electron transport in equivalent to a 2D electron wave in graphene channel [3] whose local doping can be electrostatically modulated by gate voltages. The conservation of lateral momentum along the junction yields the relative refractive index and corresponding transmission probability $T(E)$ of carrier propagation across junction [6]. Therefore, we can compute current density using following current equation:

$$\frac{I_D}{W} = \frac{2q}{h}\int dE \frac{\pi\hbar D(E)v_F}{WL} T(E)\left[f_S(E) - f_D(E)\right] \qquad (1)$$

where, I_D is current density, $D(E)$ is density of states, $T(E)$ is transmission, v_F is fermi velocity, W and L are width and length of channel, f_S and f_D are fermi distribution at source and drain, respectively.

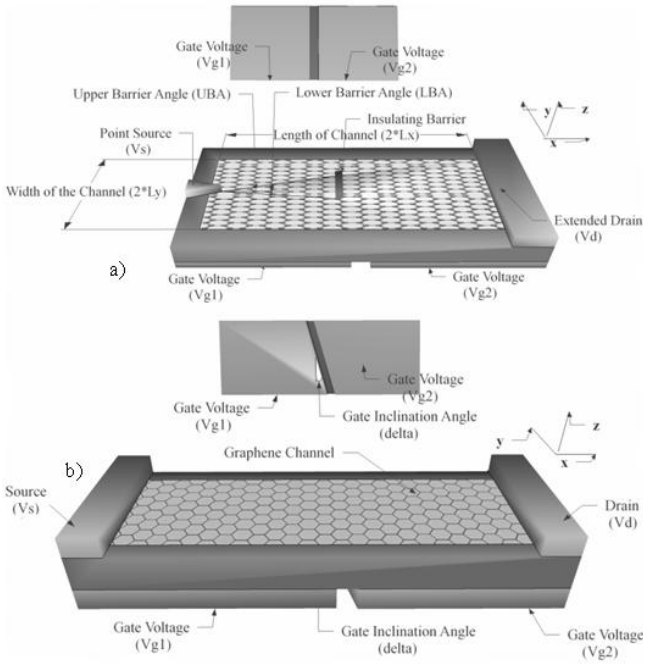

Fig. 1. Device structure of analyzed proposals for four terminal GEOT. Both induce bandgap by blocking certain energies by emulating 2-D ray optics. Graphene channel, in x-y plane, rests over substrate/dielectric. Both have two back gates, which electrostatically segment the channel into region 1 (n-side) and 2 (p-side), under V_{G1} and V_{G2} respectively, with relative refractive index η_{21} and critical angle θ_C ($\sin^{-1}\eta_{21}$). a) [6] Electron stream (circular wavefront) from point electron injection source is blocked by insulating barrier placed in the centre of the channel. Junction is formed in y-direction along the barrier. In addition, electron incident at junction with angle (θ_i) greater than θ_C is blocked. θ_B is barrier subtended at source for symmetrically placed barrier i.e. for UBA=LBA. b) [5][7] Electron injected from source (planar wavefront) is blocked from traversing from region 1 to region 2, if the critical angle of its wavefront is less than gate inclination angle (δ).

3. Results and Discussion

Table I gives the consolidated summary of the simulation results of both designs qualitatively and quantitatively. Firstly, it can be found that the study of barrier position and geometry (cf., Fig. 2) posits that transfer characteristics of two designs are similar. Moreover, for design A, minimum I_{OFF} is achieved for symmetrically placed barrier. Both designs show independence of polarity w.r.t. θ_B subtended at the source for design A, or gate inclination angle δ of design B. Furthermore, Fig. 2 also illustrates the issue of non-zero V_{G2} for I_{OFF} point. It would lead to significant reduction in the static power dissipation if the circuit were designed with an OFF-state voltage of zero.

Secondly, the effect of symmetrical widening of insulating barrier along y-axis, i.e. increasing θ_B for design A, and δ for design B. Both I_{ON} and I_{OFF} decrease with increasing θ_B (δ) because of blocking of injected electrons over a wider energy spectrum by the insulating barrier in design A, and total internal reflection in design B.

TABLE I
COMPARING BEHAVIOR OF DESIGN A WITH DESIGN B

Swept Parameter	DESIGN A	DESIGN B
Moving Barrier Position ($\pm\theta_B$) or Orientation of Gate Inclination ($\pm\delta$)	Drain Current same for designs m and n if (UBA_m,LBA_m) = (LBA_n,UBA_n) Lowest I_{OFF} and highest I_{ON}/I_{OFF} for UBA=LBA.	Drain Current same for designs m and n if ($\delta_m = -\delta_n$).
Increasing θ_B (δ)	a) Drain Current decreases. b) I_{ON}/I_{OFF} increases. c) SS decreases. d) For I_{ON} >0.1mA/um and $I_{ON}/I_{OFF} > 10^4$: nn region: 14°-21° np region: 14°-26° e) At $\theta_B = 19^o$: nn region :: I_{ON} ~ 0.15mA/um; I_{ON}/I_{OFF} ~ 11 x 10^4; SS ~ 40mv/dec np region :: I_{ON} ~ 0.28mA/um; I_{ON}/I_{OFF} ~ 20 x 10^4; SS ~ 82mV/dec	a) Drain Current decreases. b) I_{ON}/I_{OFF} increases. c) SS decreases. d) For I_{ON} >0.1mA/um and $I_{ON}/I_{OFF} > 10^4$: nn region: 16°-26° np region: 16°-36° e) At $\delta = 19^o$: nn region :: I_{ON} ~ 3.7mA/um; I_{ON}/I_{OFF} ~ 6 x 10^4; SS ~ 44mV/dec np region :: I_{ON} ~ 2.5mA/um; I_{ON}/I_{OFF} ~ 3.5 x 10^4; SS ~ 81mV/dec
Increasing Temperature	I_{ON} slightly increases.	I_{ON} slightly decreases.
Effect of V_{G1} (Equivalent for both designs)	Device Characteristic symmetrical about polarity of V_{G1}.	Device Characteristic symmetrical about polarity of V_{G1}.

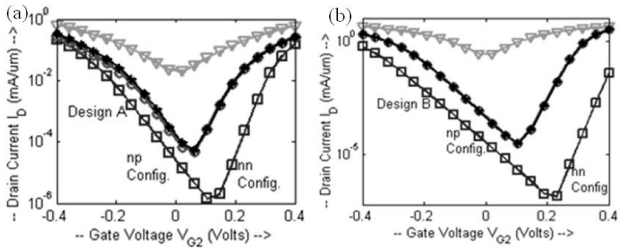

Fig. 2. Effect of moving insulation barrier of fixed dimensions along the y-axis in design A and polarity of gate inclination for design B. a) minimum I_{OFF} is achieved for symmetrically placed barrier i.e. when UBA=LBA (20° in our case) (□ marker). Drain current remains same for barrier positions mirrored about x axis along the barrier's y-axis (* overlapping with ○ marker). * represents intermediate barrier position i.e. UBA=2 LBA. b) Gate inclination (δ) in design B begets similar transfer characteristics in Graphene channel as θ_B in design A. Moreover, * (δ=+20°) overlap with ○ (δ=-20°) lines predicts functional independence of device of polarity of δ. Δ trend corresponds to absence of barrier for both a) and b).

Nevertheless, I_{ON}/I_{OFF} improves continuously because of steeper fall in I_{OFF}. In addition, SS less than 60mV/dec have been observed for θ_B (δ) > 12^0 for both architectures.

Next, we observed that as temperature increases, the leakage current (I_{OFF}) increases and SS for nn Config for both designs degrades though it remains lower than the thermal benchmark for traditional MOSFETs. However, V_{G2} corresponding to I_{OFF} remains constant. Furthermore, for

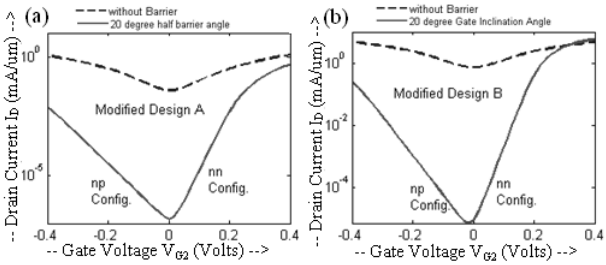

Fig. 3. Impact of chemical doping or top gate on V_{G2} translation at 300K and V_{G1}=1V. Graphene channel is doped to equivalent of V_{dope} eV or top gate is used to materialize the effect. Objective is to attain zero V_{G2} for I_{OFF} to match with switch-off for contemporary logic levels. V_{dope} is a function of θ_B (or δ), V_{G1} and gate transfer capacitance factor (β) if top gate is used for tuning. For both designs, V_{dope}=0.1345eV (solid line).

V_{G1} swept from -1V to 1V, device characteristics were found to be independent of polarity i.e. nn config ≡ pp config. Additionally, drain current reduces with increasing $|V_{G1}|$, but steeper fall in I_{OFF} improves the I_{ON}/I_{OFF} ratio.

Finally, a modification, which is applicable to both designs, is proposed to overcome the problem of non-zero V_{G2}. The channel can be chemically doped [7] to equivalent of V_{dope} or a top gate can be placed for compensation voltage V_{dope} with transfer factor 'β'. This should electrostatically shift the DOS/energy states for entire channel by βV_{dope}. Therefore, with careful tuning both designs can have zero V_{G2} for I_{OFF} point as shown in Fig. 3, thereby reducing static power dissipation. However, this improvement comes at the cost of additional terminal or increase number of fabrication steps.

4. Conclusion

The influence of device geometry, temperature and operating voltages on performance (SS, I_{ON} and I_{ON}/I_{OFF}) GEOT has been computationally investigated. Designs A and B have similar transfer characteristics and generate best response for symmetrical structures. Unipolar operation i.e. 'nn' (V_{G1}, V_{G2} > 0) or 'pp' (V_{G1}, V_{G2} < 0) is recommended to attain sub k_BT/q $\log_e(10)$ mV/dec slope for entire temperature range of interest. Design A with smaller current is better for low power devices. However, high I_{ON} and symmetrical anatomy of design B that renders its layout easier compared to the former, makes it a better architecture for VLSI. Lastly, a suitable solution has been proposed to address the issue of non-zero voltage for the I_{OFF} point.

Acknowledgments

This work at the National University of Singapore was supported by MOE under Grant. R263000689112. The authors would like to thank Dr. Tony Low for helpful discussions.

References

[1] Tura, A. et al., IEEE Transactions on Electronic Devices, vol. 57, Issue 6 (2010). [2] Neto et.al, Reviews of Modern Physics, vol. 81, Issue 1, (2009). [3] V. Cheianov et al., Science, vol. 315, Issue 5816 (2007). [4] J. Williams et al., Nature Nanotechnology, vol. 6, Issue 4 (2009). [5] T. Low et al., Phys. Rev. B, vol. 80, Issue 15 (2009). [6] R. Sajjad et al., Applied Physics Letters, vol. 99, Issue 12 (2011). [7] T. Sohier et al., Applied Physics Letters, vol. 98, Issue 21 (2011).