Estimation of metal-graphene interaction strength through quantum capacitance extraction of graphene in contact with metal

R. Ifuku, K. Nagashio, T. Nishimura and A. Toriumi

Department of Materials Engineering, The University of Tokyo
7-3-1 Hongo, Bunkyo-ku, Tokyo, 113-8656, Japan
Phone: +81-3-5841-7161, E-mail: ifuku@adam.t.u-tokyo.ac.jp

1. Introduction

Because of the small density of states (DOS) of graphene, a part of energy applied for inducing carriers in graphene will be used to excite them to higher energy states away from Dirac point. This extra-energy, expressed by $E = \frac{Q^2}{2C}$, can be dealt as capacitance (so-called quantum capacitance: $C_q$) in the equivalent circuit and is one of the quantum corrections separated from classical geometric capacitance ($\ll \epsilon/d$). Under the condition $E_F \gg kT$, $C_q$ is written in the following simple equation\cite{1},

$$C_q \approx \frac{e^2}{\pi \hbar v_F} \approx e^2 \text{DOS},$$

where $E_F$ is the Fermi energy and $v_F$ is the Fermi velocity. This equation clearly shows that DOS can be directly determined out from the extraction of $C_q$. Thus, capacitance measurement, which doesn’t include scattering process unlike transport measurement, is very useful for observing DOS of graphene.

So far, we have focused on properties of metal-graphene contacts and demonstrated that the carrier density in graphene underneath Ni electrode is modulated based on transport measurements\cite{2}. On the other hand, theoretical calculation predicted that the DOS of graphene is altered by the chemical bonding between metal and graphene\cite{3,4}. Therefore, it is important to understand metal-graphene interaction qualitatively.

The objective of this study is to estimate DOS of graphene in contact with metal through the extraction of quantum capacitance in the metal/graphene/SiO$_2$/Si stack system and to quantify the strength of metal-graphene interaction.

2. The requirement on SiO$_2$ thickness

In order to extract quantum capacitance of graphene in contact with metal ($C_q^*$), metal/graphene/SiO$_2$/Si stack system, as shown in Fig. 1(a), is selected in terms of electrical reliability of the insulator. Therefore, at first, the requirement of SiO$_2$ thickness ($d_{SiO_2}$) for experiments of capacitance measurement is discussed from the following two points.

(i) Extraction of $C_q^*$ from $C_{total}$

$C_q$ contributes to geometric capacitance in series, so other capacitance components need to be as large as possible in order to increase the ratio of $C_q^*$ to $C_{total}$. The equivalent circuit for the device (i) can be shown as Fig. 1(b), where $C_{SiO_2/Si}$ is introduced parallel to the series of $C_q^*$ and $C_{total}$.

![Fig. 1](image1)

Fig. 1 (a) Two kinds of device structures. (b) The equivalent circuit of device (i).

$C_{SiO_2/Si}$ - This is because the area of top metal is wider than that of graphene. So the ratio of $C_q^*$ to $C_{total}$ is determined by the area ratio of graphene and $d_{SiO_2}$, as calculated in Fig. 2(a). This calculation suggests that $d_{SiO_2} < ~11$ nm is required.

(ii) Visibility of graphene on very thin SiO$_2$

The SiO$_2$ thickness is also important for visible detection of graphene on SiO$_2$/Si substrates using optical microscopy, and, in this sense, $d_{SiO_2} = 90$ nm and 300 nm have been selected as substrates. However, graphene transferred on SiO$_2$ with other thickness is still visible because the contrast exits. As theoretically predicted\cite{5}, contrast becomes negative in the case of monolayer graphene on SiO$_2$ with $d_{SiO_2} < ~11$ nm. The negative value of contrast means that graphene is brighter than the substrate. Fig. 2(b) shows the calculated contrast as a function of wavelength in the case of $d_{SiO_2} < ~11$ nm by a Fresnel-law-based model\cite{3}. Because the minimum value of absolute contrast is ~0.004 in 8 bit grayscale, this calculation suggests that $d_{SiO_2} < ~5$ nm is required for the visibility and the wavelength have a negligible influence on visibility in this range.

![Fig. 2](image2)

Fig. 2 (a) $C_q^*$ contribution to total capacitance in case of $S_{graphene}$/$S_{metal}=1:2$ ($S$ denotes the area, $S_{graphene}$/$S_{metal}$=$S_{total}$). In this calculation, there has no value at $E_F = 0$ eV. $\Delta C$ represents the ratio of capacitance change: $\Delta C=(C_{total}-0.3\text{eV})-C_{total}-1.5\text{eV})/C_{total}$. (b) Calculated contrast of graphene on very thin SiO$_2$ as a function of wavelength.
3. Device fabrication

Based on the above-consideration, graphene was mechanically exfoliated from Kish graphite onto 4 nm SiO₂/n'-Si substrates. The contour and area of graphene could be exactly determined using optical microscopy not by bright-field mode but by dark-field mode. The number of layers was confirmed by Raman spectroscopy. Topgate contact metal of Au (~100 nm) was thermally evaporated directly using patterned-PMMA mask supported by a Si substrate with 200-μm□ window (Fig. 3). As there are 4 or more patterns within PMMA mask on 200-μm□ window, two kinds of capacitors can be prepared by this resist-free metal deposition process at one time: (i) metal/graphene/SiO₂/Si and (ii) metal/SiO₂/Si (Fig. 1(a)). The capacitance measurement was carried out for these two devices with Agilent E4980A.

Fig. 3 (left) PMMA mask and Si with 200-μm□ window. PMMA membrane is transferred from another Si substrate without window. (right) Optical micrograph of PMMA mask and hole patterns (size: 20×20μm and 20×30μm).

4. Extraction of quantum capacitance

The total capacitance is shown in Fig. 4(a). In addition to the capacitance contribution of n'-Si as a function of Vᵢ, detected in the device (ii), Cᵢ contribute is clearly observed in device (i). The measured capacitances are modeled as Fig. 1(b), where C₅₀₀/SiO₂/Si is series capacitance of both SiO₂ and n'-Si. In order to extract C₅₀₀, experimentally measured C₅₀₀/SiO₂/Si was subtracted twice from the capacitance of the device (i) with careful estimation of graphene’s area. Fig. 4(b) shows extracted C₅₀₀. The dotted line is theoretical prediction of C₅₀₀ as expressed in Eq. (1). Although graphene surely contacts metal and acts as one of electrodes, Fermi level of graphene was modulated by the gate voltage. Moreover, linear relation observed at |Eₜ|>0.15 eV suggests that the metal has no influence on DOS of graphene.

Next, plateau region near the Dirac point should be considered. This region is known to be attributed to the response of carriers induced externally by charged impurities at the SiO₂ surface [6], which is much larger amount than carrier induced intrinsically in graphene at the same energy. Furthermore, in the present device structure, metal-graphene interaction should be taken into consideration by a coupling strength [7]. Therefore, in order to extract the influence of charged impurities, the present data was compared with C₅₀₀ determined experimentally by Y₂O₃ topgate device [8] (Fig. 4(c)). The difference of these two devices is whether graphene contacts metal or not. In fact, the non-uniformity of the charged impurity distribution on the SiO₂ surface has to be taken into account, but this comparison could maximize the effect of the metal-graphene interaction. So it is roughly suggested that the Au-graphene interaction increased DOS of graphene near Dirac point by DOS≈1×10⁻¹⁷/eVm².

5. Conclusion

Using resist-free metal deposition process, the metal/graphene/SiO₂/Si stack was successfully fabricated and the quantum capacitance of graphene in contact with metal was extracted. Although metal-graphene interaction have little influence on DOS of graphene, especially at |Eₜ|>0.15 eV, the measurable amount of increase in DOS of graphene near the Dirac point was observed, even after the extraction of effect of charged impurities. In the case of Au, the increase in DOS by the interaction was estimated to be 1×10⁻¹⁷/eVm².

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