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3kV-class DIMOSFET on 4H-SiC (000-1)

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1. Introduction

4H-SiC silicon carbide (SiC) power devices are regarded as next-generation power devices that are expected to replace the present silicon power devices because of their potentially high performance. On the other hand, small channel mobility of gate oxides of SiC MOSFETs has been an obstacle to the commercialization of SiC power devices.

The higher the blocking voltage becomes, the higher the resistances of drift layer and JFET region become. Hence, it is considered that the influence of the poor channel mobility would be less in 3kV-class MOSFETs than in 1.2 kV-class MOSFETs. On the other hand, it has been reported that even in 3 kV-class DIMOSFET's, the channel resistance still accounts for a substantial fraction of the total resistance of DIMOSFET [1].

It has been reported that Double-Implanted MOSFET (DIMOSFET) on 4H-SiC carbon face (C-face) is a possible solution to this problem [2]. In this study, we optimized the structure of 3kV-class DIMOSFET on C-face by numerical simulation and test device fabrication.

2. Device simulation

The schematic cross-sectional view of the unit cell is shown in Fig. 1. In the present work, the model of channel conductivity was evaluated by the electric characteristics of lateral MOSFETs on C-face. The maximum mobility of these lateral MOSFETs was about 40 cm^2/Vs. The drift layer thickness was 26 μm. The doping concentration was 3.7×10^{15} cm^{-3}. The cell pitch and channel length were 10 μm and 1 μm, respectively. The gate oxide layer thickness was 60 nm. The active areas of simulated DIMOSFETs were 1 cm^2. The device characteristics were calculated with 2D device simulation.

The JFET resistance in 3 kV-class DIMOSFET tends to be higher than that in 1.2 kV-class DIMOSFET. To reduce the JFET resistance, the effect of current spread layer (CSL) was also evaluated.

Figure 2 shows the on-state characteristics of calculated 4H-SiC DIMOSFETs. The DIMOSFETs showed a specific on-resistance of 15.8 $m\Omega cm^2$ at a gate bias of 20 V and V_D of 1.5 V. Figure 3 shows the blocking characteristics of the calculated DIMOSFET. Calculations of the blocking characteristics were executed with gate-shorted source. It shows avalanche behavior and the blocking voltage of the MOSFET was 3900 V. Figures 2 and 3 also shows the impact of CSL on the electrical characteristics. The specific on-resistance was reduced to 9.9 $m\Omega cm^2$. The blocking voltage was 3800 V. The specific on-resistance of DIMOSFET with CLS on silicon face (Si-face) was also calculated to estimate the impact of C-face channel. The specific on-resistance was 11.8 $m\Omega cm^2$ on Si-face. Hence, the C-face channel and optimized CSL structure can reduce the resistance of MOSFETs with the blocking voltage.

3. Device Fabrication

The chip size of fabricated DIMSOFETs was 1.9 mm×1.9 mm. The active areas of these DIMOSFETs were 0.82 mm^2. The DIMOSFETs were fabricated on two types of C-face n-type 4H-SiC wafers. The drift layer thickness of Sample A was 26 μm. The doping concentration was 3.7×10^{15} cm^{-3}. Sample B has an additional CSL layer on 26 μm drift layer. The cell structure was hexagonal cell whose pitch and channel length were 10 μm and 1 μm, respectively. The p-well structure and the source region were formed by aluminum ion implantation and phosphorus ion implantation, respectively. The termination structures and p++ contact regions were also formed by aluminum ion implantation. Activation annealing of implanted ions was executed at 1700 °C for 5 min. The gate oxide layer thickness was 60 nm and phosphorus-doped polycrystalline silicon gates were formed

on the layer. The ohmic contacts were formed by aluminum and nickel depositions followed by annealing at 1000 °C for 2 min.

Figure 4 shows the on-state characteristics of the fabricated MOSFETs. Sample A showed a specific on-resistance of 15.5 mΩcm^2 at a gate bias of 20 V. Sample B showed a specific on-resistance of 10.5 mΩcm^2 at a gate bias of 20 V. These results show CSL layer was effective for reducing the specific on-resistance. The blocking voltages of samples A and B were 2670 V and 2480 V, respectively. Measurements of the blocking characteristics were carried out with gate-shorted source. The degradation of blocking voltage might be due to JTE structures.

These results suggest that 4H-SiC DIMOSFETs on C-face with CSL structure can realize low on-resistance power MOSFET comparable to devices previously reported.

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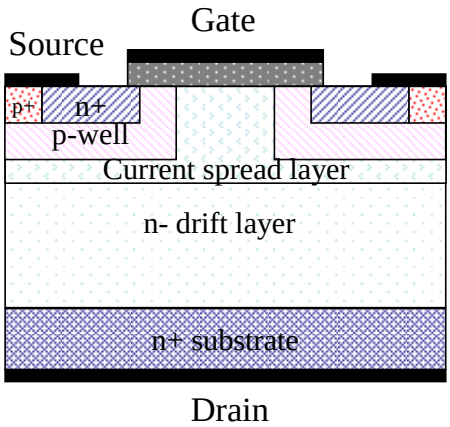

Fig.1 Schematic cross-section of DIMOSFET.

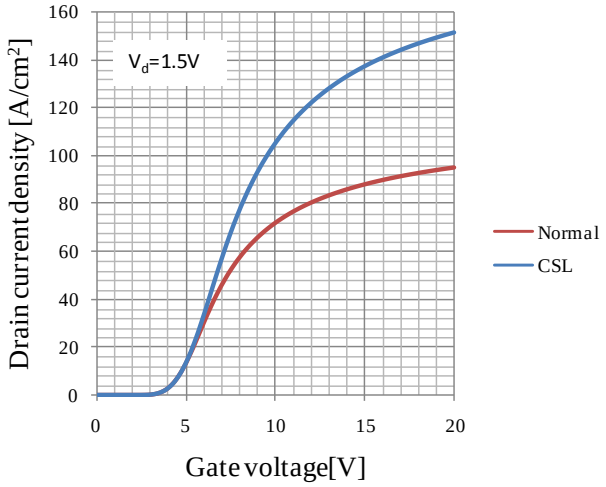

Fig 2. The on-state characteristics of calculated SiC-DIMOSFET.

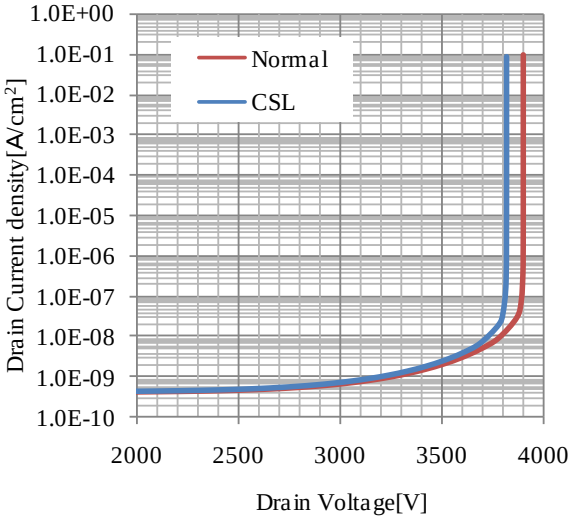

Fig3. The off-state characteristics of calculated SiC-DIMOSFET.

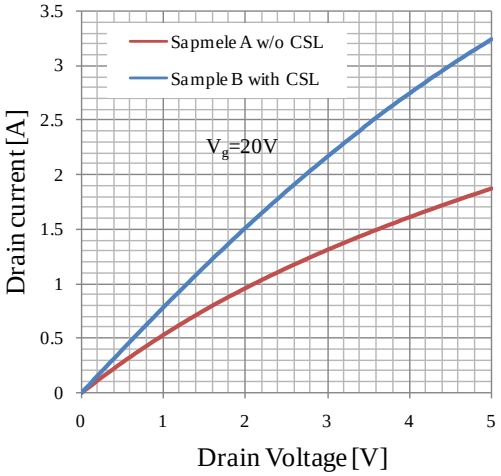

Fig 4. The on-state characteristics of the fabricated MOSFETs.