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Modeling of the Impurity-Gradient Effect in High-Voltage Laterally-Diffused MOSFETs

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Abstract

The MOSFET capacitances in high-voltage laterally-diffused MOSFET, where its channel impurity concentration tails off along the channel from source side to drain side, are investigated. This pertinent doping inhomogeneity leads to an additional electrostatic contribution to the amount of internal charge. With an emphasis on the deviations from homogeneous dopant-profile settings, the additional contribution was formulated within the framework of MOSFET compact models based on the surface potential description. This approach is found successful for all Vds values, where the resulting high-voltage MOSFET specific features are observed.

1. Introduction

A compact model seeks literally a "compact" description of its target device, maintaining engineering-level accuracy and providing computational efficiency in contrast to TCAD. The present generation of compact MOSFET models relies on a description with the surface potential, believed most correct, typically at as few as two locations within a MOSFET; one at the source/channel boundary and the other at the channel/drain boundary. All important, electrical quantities of the MOSFET derive from these surface potential values. The industry-standard high-voltage MOSFET model HiSIM_HV has been developed based on the surface-potential concept [1, 2].

The laterally-diffused MOSFET (LDMOS) is a high-voltage MOSFET, where the channel impurity concentration tails off along the channel from source side to drain side (see Fig. 1). This pertinent inhomogeneity causes notable changes of the electric characteristics [3], on which we are focusing with the reported modeling effort. In light of the usages of high-voltage MOSFETs, primarily for analog-precision circuitry and power switching, large attention has been paid to DC as well as AC characteristics, particularly, when the drain current is near Vds=0.

This work focuses on the notable LDMOS capacitance characteristics changes for Vds > 0 (see Fig. 2). TCAD was utilized for generating capacitance-voltage (C-V) curves, instead of actual measurement, for obtaining access to the internal LDMOS quantities such as potentials at the same time. A close analysis of the TCAD-simulated results leads to a new improved formulation of capacitances within the framework of the HiSIM_HV2.0.0 compact model.

2. Modeling of Effects Caused by Impurity Gradient

TCAD simulation revealed notable Vds-dependent characteristics changes in the capacitances as can be seen in the gate capacitance Cgg shown in Fig. 2. In the presence of applied Vds, the Cgg capacitance curves develop a peak, which varies in shape for different Vds. It was once believed that this peak is caused by the impurity gradient [4], which was found to be incorrect [3]. The separate effect of an inhomogeneous impurity concentration has been extracted from the difference of Cgg simulations (TCAD) with a doping gradient and without (see Fig. 2, *right pane*). It is found that the impurity gradient induces an additional effective charge in the channel, which can be described as

$$C_{\mathrm{gd\_grad}} = C_{\mathrm{gd\_uni}} + \frac{d\Delta Q_{\mathrm{ce}}}{dV_{\mathrm{ds}}} \tag{1}$$

where ΔQce is the difference of the amount of the total induced internal charge.

Fig. 4 shows the exhibited differences in the potential distribution along the channel associated with the induced internal charge. The effect on the potential is strongly enhanced at Vgs=Vds=0, and the origin of the induced charge is attributed to this change of the potential distribution. The drain current itself has been verified to be correctly modeled by the averaged impurity concentration [3]. Therefore, the focused task to be solved is the modeling of ΔQce, which is done using the Gauss law, resulting in

$$\Delta Q_{\mathrm{ce}} = \varepsilon_{\mathrm{si}}(E_{\mathrm{grad}} - E_{\mathrm{uni}}) \cdot W \cdot depth \tag{2}$$

where $\varepsilon_{\mathrm{si}}$ is the silicon permittivity, W is the device width, and *depth* is the depth until which the additional field is induced. E_{grad}, E_{uni} and *depth* are calculated from the potential difference between the source side and the drain side.

As HiSIM_HV solves internally the Poison equation at the source side and the drain side independently, the impurity gradient can be easily incorporated. With the use of the two surface potentials, ϕ_{S0} and ϕ_{SL}, as solutions of the Poisson equation, the strength of the electric field induced along the channel, E_{grad}, is written as

$$E_{\mathrm{grad}} = \frac{\phi_{\mathrm{SL}}(\mathrm{uniform3}) - \phi_{\mathrm{S0}}(\mathrm{uniform1})}{L} \tag{3}$$

where L is the channel length. The different impurity concentration at the soruce side and the drain side results in different Vgs responses, namely different potential bendings. The total electric field induced in the channel is $E_{\mathrm{grad}} + E_{\mathrm{uni}}$ where E_{uni} is the field under a homogeneous impurity profile conventionally considered written as

$$E_{\mathrm{uni}} = \frac{\phi_{\mathrm{SL\_U}}(\mathrm{uniform1}) - \phi_{\mathrm{S0}}(\mathrm{uniform1})}{L} . \quad (4)$$

The anomalous Cgg charactersitcs observed in LDMOS (see Fig. 2) is determined not only by the intrinsic MOSFET charactersitics but also by those of the overlap region between gate and drift region. The overlap region is also strongly influenced by the potential value ϕ_{SL} at the drain side. The increase of ϕ_{SL} at the drain side of the intrinsic MOSFET due to the impurity gradient causes a reduction of the resistance effect in the high resistive drift region (see Fig. 1). Consequently, to capture all the effects caused by the impurity gradient, the different impurity concentrations at the source side and the drain side must be explicitly considered in solving the Poisson equation. Figure 4 shows the comparison of calculated Cgg with and without the dopant gradient between the developed compact model and TCAD results. Good agreement reveals the accuracy of the developed compact model. The potential values ϕ_{S0} and ϕ_{SL} calculated by HiSIM_HV with inclusion of the impurity gradient are depicted in Fig. 3 for comparison.

3. Conclusions

The capacitance enhancement for Vds>0 was described and modeled within the framework of compact models using the surface potential descriptions. This approach is found successful for Vds > 0, just as was for Vds =0, resulting in further improvement of the surface-potential compact modeling of high-voltage MOSFET for circuit simulation.

References

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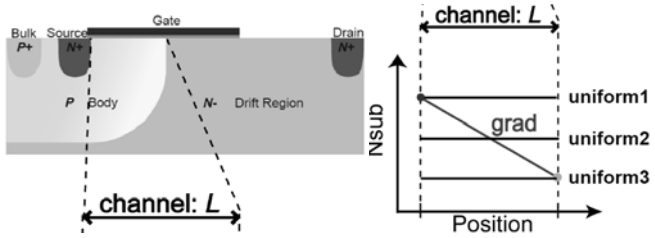

Fig. 1. Investigated device structure and channel impurity profiles ("grad", "uniform1", "uniform2", "uniform3"). In the "grad" profile, the channel impurity concentration is set to decrease by one-decade along the channel from the source to the drain, and "uniform2" is the averaged impurity concentration.

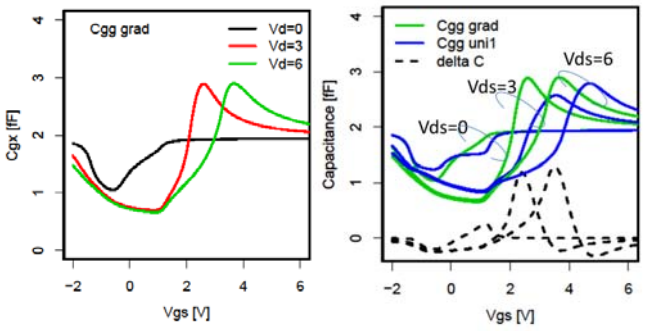

Fig. 2 Calculated capacitances Cgg with respect to the gate voltage, together with Vds=0, 3, 6V, using 2-D device simulation (TCAD). Cgg for different profiles ("grad" and "uniform1") and the difference between them (right).

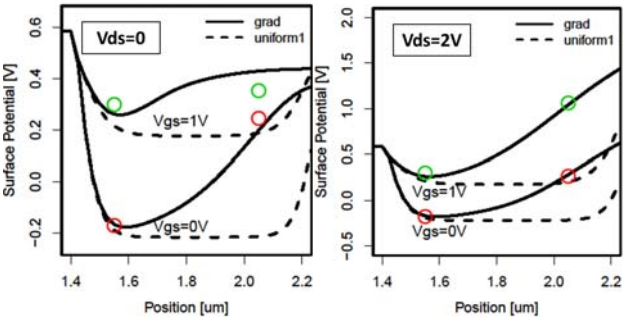

Fig. 3 Potential profile along the MOS interface, calculated using TCAD, for two different impurity profiles ("grad" and "uniform1"). The "grad" profile exhibits a potential drop within the channel even at Vds=0 (left). Marks are the potential values ϕ_{S0} and ϕ_{SL} calculated by HiSIM_HV with inclusion of the impurity gradient.

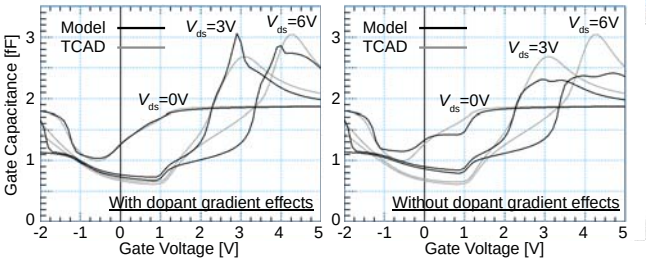

Fig. 4 Cgg (=Cgs+Cgb+Cgd) is plotted and compared with the "measurement" (TCAD-generated) curves, at Vds=0, 3, and 6 V, for the "grad" profile. Without inclusion of the impurity gradient term, the capacitance peak at higher Vds becomes not as outstanding as the measurement exhibits.