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Parasitic Bipolar Effect of a Thin-film SOI Power MOSFET in High Temperature

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Abstract

This paper describes the parasitic bipolar effect of the thin-film SOI Power MOSFET in high temperature. This effect appeared in on-state was suppressed as temperature increased. This effect appeared in off-state promoted as the temperature increased. This reduced the breakdown voltage.

1. Introduction

High temperature applications of the power devices and power ICs have been attracting attention because of increasing the demand of automotive, jet engine for aircraft, space exploration, and deep oil / gas extraction applications. Silicon on insulator (SOI) technology is emerging as the most mature solution for these fields [1] because of lower leakage current as well as high reliability (immunity of temperature induced latch up). Thin-film approaches are quite promising because it showed lower leakage current. As a results, SOI circuits can operate at temperature above 573K, while bulk devices are usually limited to 423K [2]. The parasitic bipolar effect is one of the key issues for SOI power MOSFETs, especially, thin-film approach[3]. In such a scheme, this paper investigates the parasitic bipolar effect of the thin-film SOI power MOSFET over the wide temperature range based on the experimental results.

2. Device structure and Fabrication process.

The schematic cross section of the fabricated thin-film SOI power MOSFET is shown in Fig.1 [4]. The body contacts were formed to suppress the parasitic bipolar effect [4] and the main structural parameters are listed in Table 1. The thin-film SOI power MOSFET was fabricated using 0.5μm-rule polycide gate process with LOCOS isolation. The device characteristics used in this investigation are listed in Table.2.

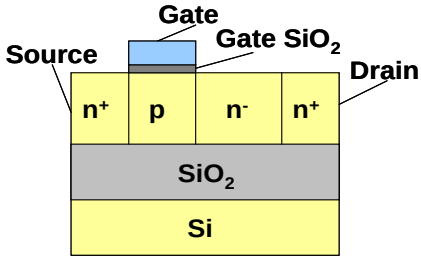

Fig.1 Schematic cross section of SOI power MOSFET.

Table.1 The main structural parameters.

Top Si layer (μm)	0.14
Buried oxide (μm)	0.4
Gate oxide (nm)	20
Channel Length (μm)	0.5
Body contact pitch (μm)	10,20,40
Drift Length (μm)	1.5
Impurity concentration in drain offset region (cm^{-3})	1.6×10^{17}

Table.2 The characteristics of the device in this measurement.

	Room temperature	573K
Threshold voltage(V)	0.60	0.24
On-Resistance(Ω・mm) *	5.47	11.8
Leakage current(A) **	2.81×10^{-12}	4.45×10^{-7}
Breakdown voltage(V) ***	14.6	8.8

*Vg=5.0(V) **Vd=6.0(V) ***Vg=0(V)

3. Result & Discussion

Subthreshold characteristics of an SOI power MOSFET are shown in Fig.2. The drain bias voltage is 6.0V. The threshold voltage decreases with increasing temperature. On/Off ratio is about 3 orders of magnitude at 573K. The SOI power MOSFET can operates at 573K. There is a hump caused by the parasitic bipolar effect at 300K and 373K. While, it disappears over 423K. The parasitic bipolar effect are suppressed over 423K.

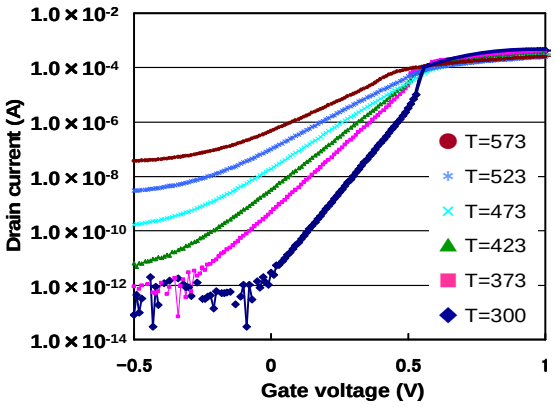

Fig.2 Threshold voltage characteristics of SOI power MOSFET for each respective temperature at Vd=6.0(V).

Dependence of the drain conductance on the drain voltage is shown in Fig.3. The gate bias voltage is 1.0V. The drain conductance increases with increasing the drain voltage and it decreases with increasing temperature. The drain conductance of 523K and 573K are almost the same. These results mean that the parasitic bipolar effect is suppressed as the temperature increases when the temperature is less than 523K.

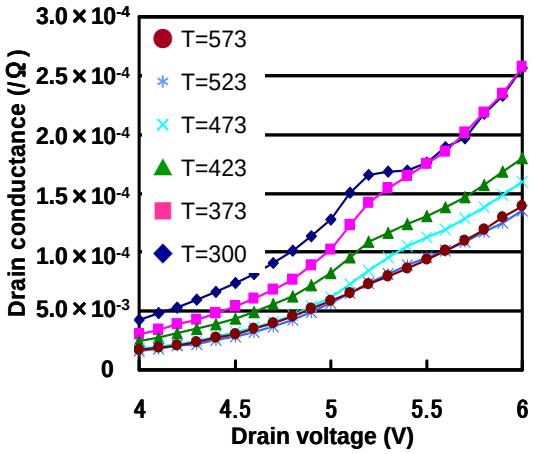

Fig.3 Dependence of the drain conductance on the temperature at Vg=1.0(V) and Vd=1.0(V).

Dependence of the on-state breakdown voltage on the temperature is shown in Fig. 4. The gate bias voltage is 1.0V. The on-state breakdown voltage slightly increases with increasing the temperature when the temperature is less than 473K. The breakdown voltage slightly decreases when the temperature is more than 473K and body contact spacing are 20μm and 40 μm. The on-state breakdown voltage of the power MOSFET with body contact spacing of 40 μm is lower than that with smaller body contact pitch at room temperature. However, when the temperature increases, the on-state breakdown voltage is almost the same regardless of the body contact pitch.

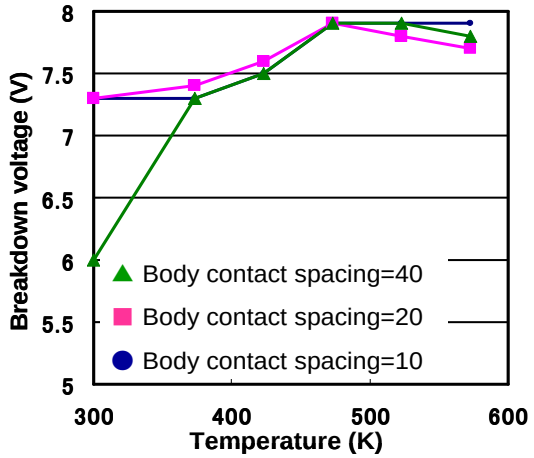

Fig.4 Dependence of the breakdown voltage on the temperature at Vg=1.0(V).

Dependence of the off-state breakdown voltage on the temperature is shown in Fig. 5. The gate bias voltage is 0V. The off-state breakdown voltage decreases with increasing temperature when the temperature is more than 400K because the parasitic bipolar effect is promoted as the temperature increases. In this case, the parasitic bipolar effect is caused by leakage current.

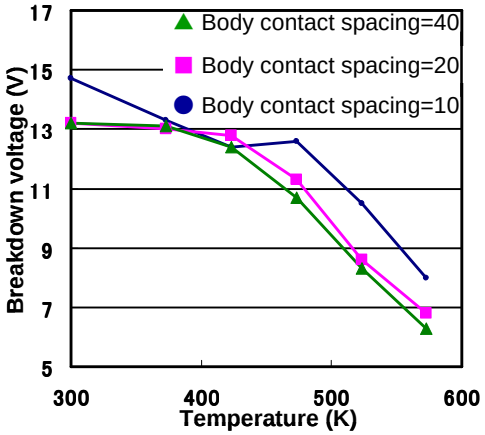

Fig.5 Dependence of the breakdown voltage on the temperature at Vg=0(V).

4. Conclusions

The parasitic bipolar effect of the thin-film SOI power MOSFET was investigated over the wide temperature range (from room temperature to 573K). This effect appeared in on-state was suppressed as temperature increased. This effect appeared in off-state promoted as the temperature increased. This reduced the breakdown voltage.

References

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