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Investigation of BTI degradation in LDMOS transistors

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1. Introduction

Integration of high-voltage devices into Complementary Metal-Oxide-Semiconductor (CMOS) process is useful for lower cost and more functions on a single chip. Laterally Diffused MOS (LDMOS) transistors are the most suitable devices for CMOS process. Many attentions are paid to the reliability of LDMOS transistors. However, most of them are focused on Hot-Carrier-Injection (HCI). [1-2]

In this paper, we have evaluated Bias Temperature Instability (BTI) and its degradation with measuring Charge-pumping-current (Icp) before and after BTI stress in LDMOSs.

2. Experiment

We have evaluated negative and positive BTI (NBTI and PBTI) degradation in P-type LDMOS (pLDMOS) and N-type LDMOS (nLDMOS) thorough measuring Icp and on-resistance (Ron). The measured LDMOS have a drift region with Shallow-Trench-Isolation (STI) manufactured with 0.18μm CMOS compatible technology as shown in Fig. 1. L_{CR}, L_{AR}, and L_{DR} show length of channel region (CR), accumulation region (AR), and drift region (DR). In this measurement we test three types of L_{CR} for pLDMOS and one L_{CR} for nLDMOS.

Schematic illustration of Icp measurement method for LDMOS transistors is shown in Fig.2. The measured Icp indicate number of interface trap (Nit). [3] Stress bias on the gate is 7.3MV/cm and temperature is 125 degrees centigrade on BTI stress.

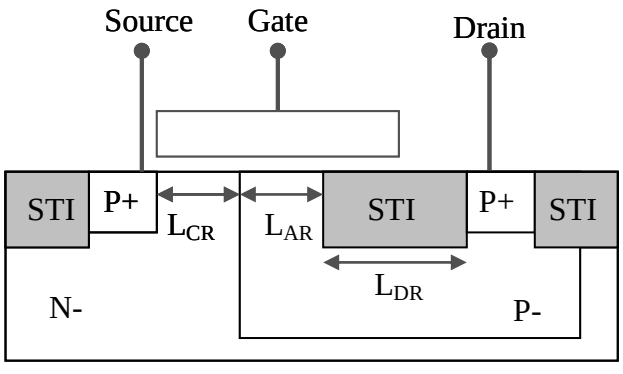

Fig. 1 Cross section of pLDMOS.

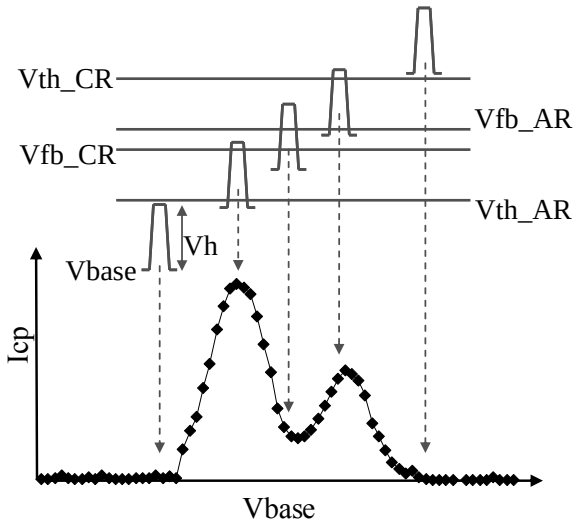

Fig. 2 Schematic illustration of Icp measurement method for LDMOS transistors. This shows relationship between pulse, threshold voltage (Vth) and flat-band voltage (Vfb) for CR and AR. Amplitude of pulse (Vh) on Icp measurement is constant

3. Result and Discussion

We have measured Icp on two conditions. One is on the source and drain connected to VSS. Another is only on source connected to VSS and drain left floating. This measurement has performed with varying Vbase and Vh for isolating Icp contribution on CR and AR. Fig. 3 shows Icp curves measured with (a) drain connected to VSS and (b) drain left floating in pLDMOS before and after BTI stresses. This results show that both Ron and Icp increase after BTI stress. In measurement condition (a), Icp on CR and AR is observed. In measurement condition (b), Icp on CR is observed. This measurement archives isolating contribution on CR and AR clearly from comparison between Fig. 3(a) and (b).

Shown in Fig. 4 and Fig. 5 are L_{CR} dependences of Icp-density shift on CR and delta-Ron by BTI stressed. Icp-density and its degradation on CR are independent of L_{CR} for pLDMOS as shown in Fig. 4. Large amount of Ron shift has been observed at large L_{CR}. BTI degradation on CR is more sensitive than that on AR.

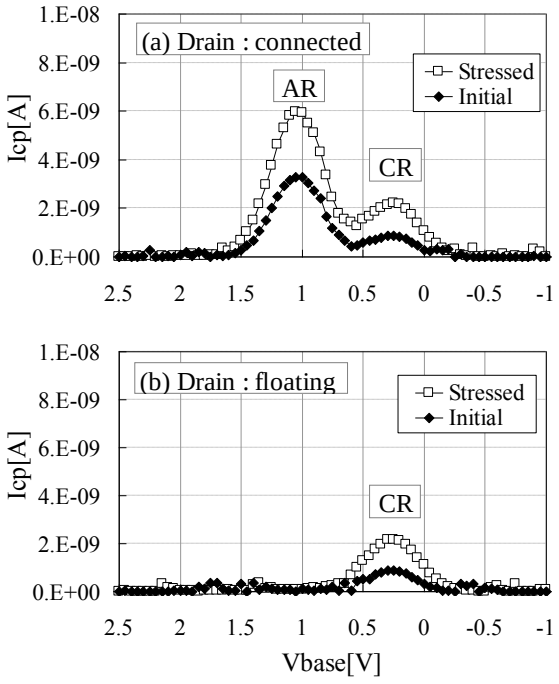

Fig. 3 Typical Icp curves measured with (a) drain connected to VSS and (b) drain left floating in pLDMOS.

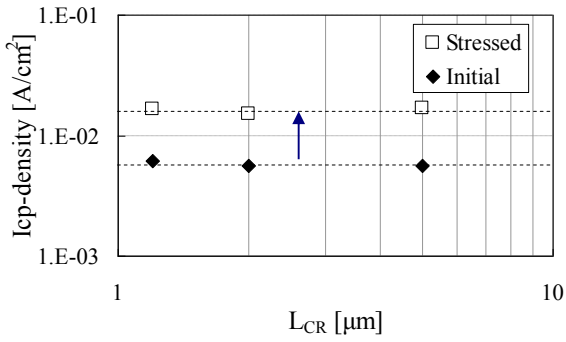

Fig. 4 L_{CR} dependence of Icp-density shift on CR in pLDMOS.

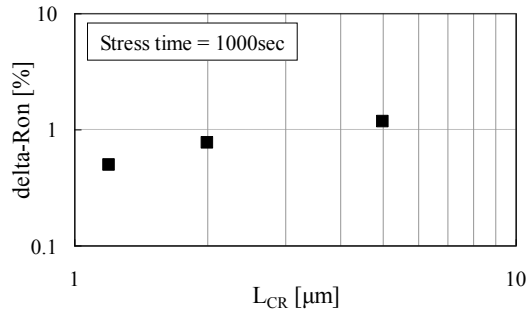

Fig. 5 L_{CR} dependence of delta-Ron shift in pLDMOS.

Delta-Icp shifts in pLDMOS and nLDMOS transistors are shown in Fig. 6. Extracted slopes are about 0.3 that is consistent for NBTI both in nLDMOS and pLDMOS. The slopes are 0.9 that is consistent for PBTI on CR and AR in nLDMOS. These results have indicated that the slopes are independent of well type. PBTI degradation mechanism is different from NBTI for CR and AR. BTI degradation mechanism is determined not by well type, but by stress polarity.

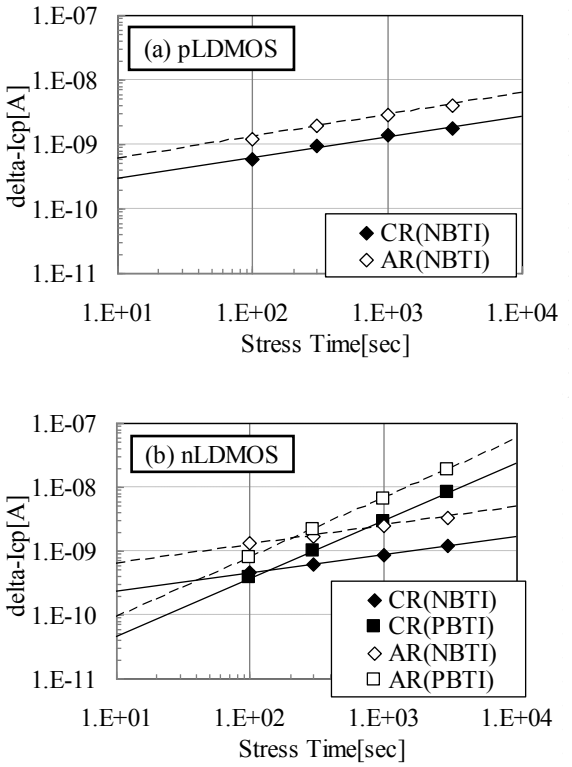

Fig. 6 Delta-Icp shifts in (a) pLDMOS and (b) nLDMOS under NBTI and PBTI stress.

4. Conclusions

BTI degradation in LDMOS transistors is investigated. It was found that L_{CR} is the effective layout parameter for pLDMOS. BTI degradation mechanism is determined not by well type, but by stress polarity.

References

[1] P. Moens et al., IEEE Trans. on Electron Devices **51** (2004) 623.

[2] J. F. Chen et al., IEEE Trans. on Device and Materials Reliability **9** (2009) 459.

[3] P. Heremans et al., IEEE Tran. on Electron Devices **36** (1989) 1318.