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Nano-textured photonic crystal light-emitting diodes and solar cells

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1. Introduction

The Si-based photonic device such as light-emitting diode (LED), photo-detector, and solar cell have been developed and attract a lot of attention recently, using the p-i-n tunneling diode structure [1] and metal-insulator-semiconductor (MIS) tunneling diode structure [2]. Whether what kind of different structures are used, two main issues are still needed to investigate. One is the improvement of the optic-electric transformation efficiency. Another is the capability to modulate the light-emitting and detection wavelength for different industrial applications. In our previous work, we demonstrate the radiative recombination rate [3] for the optic-electric transformation efficiency can be enhanced greatly with the melt of Ge in Si photonic devices. The wavelength of the light emission and detection can also be further adjusted due to the change of the material band-gap [4-6]. Besides the SiGe material, the nano-textured surface structure with the photonic crystal effect [7-10] is also found to be another method to change the characteristics of material for the different applications. In this work, we develop the nano-scale surface textured Si LED and solar cell. For the application of LED, the higher light-emission efficiency (~10X) and the capability to extract the special light emission wavelength is successfully demonstrated. For the application of solar cell, the characteristics of top textured solar cells is developed and estimated to see if the structure is worthy to be scaled from the modern micro-meter (um) level down to the nano-meter (nm) level continuously. The process of nm-scale textured Si optoelectronic device used in this work is fully comparable to the modern CMOS industry [11-12].

2. General Instructions

Fig. 1 shows the sketch and detailed process flow for proposed nm-scale textured Si LEDs and solar cells studied in this work. We use the standard shallow trench isolation (STI) process used in the CMOS technology to manufacture the nm-scale textured structure on the Si photonic devices. The detailed process condition can be referred to Ref. 11 and 12.

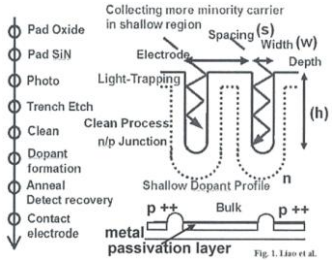


Fig. 1. The schematic diagram of the nm-scale trench structure for the application of Si LED and solar cell.

It starts with the growth of a silicon oxide film on the bare Si <100> wafer with the resistivity about 1 ohm-cm; a thick Pad-SiN layer (~40 nm) is further deposited to do the anti-reflection layer. After the photo deposition and wet etching, the nm-scale trench structure on the top surface is formed. It can collect more minority carrier, enhance the light-trapping effect, reduce the reflectivity of the cells, and finally result in the larger optic-electric transformation efficiency. The surface trench depth and width are 300 nm and 30 nm, respectively, with different trench spacing from 100 nm to 1 μm in order to study the surface plasma and photonic crystal effect with different spacing distance. The surface area (A) of the tested Si photonic device is about 1 cm^2. The front contact metal is evaporated by the Al/Ti/Pd/Ag metal and is thickened by the electroplating. The grid distance on the wafer surface for the solar cell device is about 0.2 cm with 4 fingers and the degree of shading can be greatly reduced. The backside surface exhibits a local P diffusion (Rsheet ~10 ohm/sq), and is covered with an 80 nm thick thermally passivated SiO_2 layer and thick low resistance Al backside contact layer.

Fig. 2 shows the electroluminescence (EL) spectra on the Si LED with and without the surface nm-scale textured structure. The drive current for the device is 100 mA at the voltage of 2V. Compared with the spectra of control Si LED with the plane surface shown in Fig. 2, it can be found that the high infrared emission intensity at ~ 1100 nm can be observed and extracted specifically with the photonic crystal effect in the nm-scale textured Si LED. The trench spacing is about 1 μm.

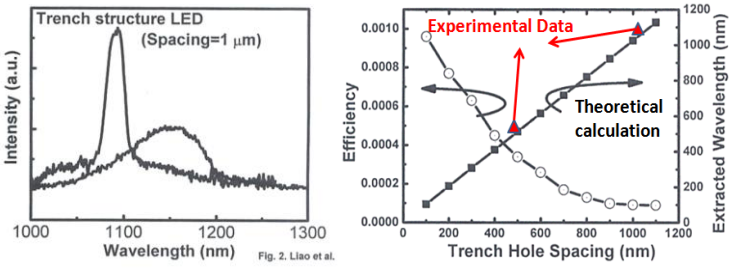


Fig. 2. The electroluminescence spectra from Si LED with and without nm-scale textured surface structure. The high light emission intensity enhancement and obvious photonic crystal effect to extract the special light emission wavelength are observed.

Fig. 3. The light-emission efficiency and extracted wavelength with different textured structures by surface plasma effect for Si MIS LED.

Besides the incorporation of Ge in the Si-based LEDs to change the band gap of the material, reported by our group previously [4-6], the different surface nm-scale

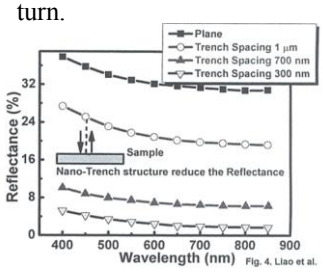
textured structures with the designed pattern spacing (Fig. 3) are demonstrated to have the high capability to extract the special wavelength of the light emission due to the surface plasma and photonic crystal effect, and the light emission efficiency can also be improved greatly (Fig. 2 and Fig. 3).

The reason for the enhanced light emission efficiency is that the more minority carrier, accumulated along the nano-scale trench structure, recombines with the majority carrier to do the more light emission. The experimental results for the special wavelength extraction and the improvement of the efficiency with different photonic crystal structures in Si LED agree well with the theoretical calculation on the response of the surface plasma effect, calculated by our previous work [13]. The surface plasma conservation law is followed by

$$\lambda = d(i^2 + j^2) \times n_d$$

where λ is the wavelength of the extracted light emission. d is the spacing of the nm-scale textured. i and j are the integer number for the plasma node. n_d is the index of the refraction (1.47 for Si).

For the application of the nano-surface structure for the Si solar cell, the reflectance with different surface structures at the wavelength between 300 nm- 900 nm are detected firstly (Fig. 4). Compared with the plane surface structure, the reflectivity of nano-scale textured can be reduced about 22 % from ~30 % to 8 %. With the optimal nm-scale surface structure design, the reflectance can be continually reduced and the solar cell efficiency should be further improved. In this work, we demonstrate that it is worthy to scale the dimension of the surface textured structure from the micro-scale, used in the current solar cell industry, to the nm-scale nm textured pattern structure, proposed in this work. The lower reflectance in the nano-scale structured surface structure is due to the much light trapping. On the other hand, the additional of SiN antireflection coating can further reduce the overall reflection about a few percent. It can enhance both short-circuit current (Jsc) and open-circuit voltage (Voc), which will further improve the final solar cell efficiency in turn.



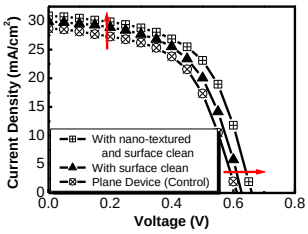


Fig. 4. The measured reflectance spectra between 400 nm and 900 nm on the Si with different surface structure treatment.

Fig. 5. The typical current-voltage (I-V) characteristics for the plane and nano-scale textured solar cell under the illumination by AM 1.5.

Fig. 5 shows the typical current-voltage (I-V) characteristics for the plane and nano-scale textured solar cell under the illumination by AM 1.5. The parameters of the total solar cell are Voc=0.61 (0.66) V, Jsc=28.7 (30.89) mA, Fill Factor (FF)=0.7 (0.73), and efficiency=12 (14.9)% for the plane (nm-textured device with additional surface clean) solar cell. The higher Jsc in the nano-level structure is due to the larger n/p junction area where can collect more carriers. Higher source current (I_L), resulted from the excitation of excess carriers by the solar radiation and low diode saturation current (I_S), reduced by the better n/p junction formation and surface clean process results in the better Voc device performance and solar cell efficiency. The highest solar cell efficiency in this work are observed and achieved to 14.9% (~2.9% higher than our control base-line) with the nano-scale textured structure (~1.9% contribution) and surface clean process (~1% contribution) such as HF dip, APM, and SPM treatment. In this work, we demonstrate the opportunity for the efficiency enhancement of the nano-scale structure solar cell successfully. The proposed process is fully comparable with the standard CMOS technology process. Even the modern multi-vertical junction solar cell in the industry is on the order of m level and our proposed process could be too expensive for the real manufacture in the modern Si solar cell industry, the nm-scale textured trench solar cell structure is still worthy to continuously develop and scale down to get the lower reflectance and better efficiency, based on our study in this work.

3. Conclusions

The optimal Ge concentration in SiGe-based solar cell has been investigated qualitatively by the systemic experiment and theoretical calculation. With the appropriate addition of Ge to a SiGe-based solar cell, the short current density is successfully increased without affecting the open-circuit voltage and then the overall efficiency is successfully improved about ~4% than the control Si solar cell. The energy band-gap of SiGe, the important parameter for the design of SiGe-based solar cell, at different temperatures is extracted by the proposed electron-hole plasma (EHP) model in the EL spectra. In addition to the advantage of the cell efficiency improvement, the $Si_{0.9}Ge_{0.1}$ solar cell has also been observed that it has less operated temperature sensitivity than Si solar cell for the real application.

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