Investigation of Electrical Performances for n-MOSFET Devices Integrating with Bonding and Thinning Technologies in 3D Integration

Chuan-An Cheng¹, Cheng-Hsien Lu¹, Chia-Hua Ho², Kuan-Neng Chen¹*  
¹Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan  
²National Nano Device Laboratory, Hsinchu 300, Taiwan  
*Tel: +886-3-5712121 ext 31558; E-mail: knchen@mail.nctu.edu.tw

Abstract
This study investigated the effects of bonding and thinning technologies on n-MOSFET devices. By presenting an evaluation of electrical performances of devices after key technology fabrication of 3D integration, the results indicate that these 3D technologies can be integrated with 0.35 μm technology node devices without degradation, showing the feasibility of 3D IC applications.

Introduction
Significance of three-dimensional integration circuit (3D IC) has been addressed in extending Moore’s law, which was obeyed in the decades for conventional integrated circuits on planer wafers. Due to the limitation of processing technologies in physical aspect, three-dimensional integrated circuits is one of the option to clear up the restrictions in scaling technology node in devices. For vertical stacking structure of a 3D integration platform, wafer level bonding, wafer thinning, and through silicon via (TSV) are three key technologies [1]-[2].

Among these key technologies, thermal compression bonding can achieve strong bond strength during stacking. The prior art has shown that the optimized Cu bonding temperature need to be higher than 350°C and the bonding time longer than 30 minutes [3]. Furthermore, thinning technology ability directly determines the TSV size [4]. However, the effects of bonding and thinning technologies need to be studied. This paper presents the investigation of effects of bonding and thinning key technologies integrated with n-MOSFET devices.

Experiments
The cross-sectional schematic diagram of n-MOSFET device is shown in Figure 1, where the gate length/width ratios are 0.35μm/10μm and 1μm /10μm. Since thermal compression bonding process combines heating temperature with pressing force, to investigate whether the electrical performances of devices will be degraded after wafer bonding process, three studies were designed for measurement, including reliability of regular devices, bonding temperature study, and bonding force study. Since bare silicon wafer does not bond with device substrate under the bonding temperature and pressure range used in this research, the device substrate was bonded with a bare silicon wafer to simulate bonding process, which can avoid the de-bonding process and be repeatable for multiple measurements for devices under different bonding conditions.

In addition, thinning process was performed from the backside of device substrate. In order to prevent moisture issue on devices, we performed a temporary bonding between device substrate and a glass as a capping layer by heating glue. The thinned device substrates were then tested to investigate after removing the capping layer. The thickness of thinned substrates was measured by spiral-micrometer. All electrical characteristics were measured by HP4156C.

Results and Discussion
The reliability of regular devices without bonding process was tested at room temperature or after 200°C annealed 4 cycles. Figure 2 shows the comparison of threshold voltages (V(th)) and variation, which indicate the electrical properties remain stable after cycling test. To distinguish the effects of temperature and force devices during thermal compression bonding, devices in the bond temperature study has no bonding force applied under different bond temperature, including room temperature, 200 °C, 250 °C, 300 °C, 350 °C and 400 °C. Figure 3 shows the electrical performance of the two types of devices under different temperature. The V(th) variation has no obvious shift in Figure 4. Therefore, it is suggested that electrical properties are maintained in the same order under 400 °C.

The bonding force study was to in the same bonding temperature with different bonding force, 0Pa, 0.5x10⁵ Pa, 1.5x10⁵ Pa and 2.5x10⁵ Pa, stressed for 50 minutes. Figure 5 shows that the measurement results under different bonding temperature and bonding force, having same curving tendency. The detailed V(th) and V(th) variation from all measurements are shown in Figure 6. We can conclude electrical performances are not changed under different bonding force and bonding temperature.

Since thinning process will affect the final TSV size directly, it is important to investigate effects from thinning process [4]-[5]. The complete V(th) and V(th) variance of device with different thickness, including 690μm, 651μm, 597μm, 554μm, 508μm and 466μm, are shown in Figure 7. It shows that devices have no degradation phenomenon after thinning process down to 466μm.

Conclusion
In this paper, two types of n-MOSFET devices were investigated after bonding and thinning processes. The V(th) variance can be always kept below 3% after wafer bonding process, for bond temperature from room temperature to 400°C and for bond force from 0 Pa to 2.5x10⁵ Pa. Furthermore, it is also found that the electrical properties do not change after thinning process for the thickness down to 466μm. From the results, we demonstrate that the optimized bonding and thinning technologies can be integrated with n-MOSFET devices in 0.35μm technology node for
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References


Fig.1 Schematics of cross-sectional structure of n-MOSFET device

Fig.2 $V_t$ and $V_i$ variance of devices after cycling tests

Fig.3 Electrical performances of the two types of devices under different temperature, including room temperature, 200°C, 250°C, 300°C, 350°C and 400°C

Fig.4 $V_t$ and $V_i$ variance of devices under different temperature with 0 Pa bonding force

Fig.5 Electrical performance of the two types of devices under different temperature and bonding force

Fig.6 $V_t$ and $V_i$ variance of the two types of devices under different temperature and bonding force

Fig.7 $V_t$ and $V_i$ variance of the two types of devices with different thickness