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RF Inductors on Nanocrystalline Silicon Passivated HR-Si Substrates

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1. Introduction

Passive devices on the low-resistivity silicon (LR-Si) substrate that is used in standard CMOS processes have high-loss performance resulting from substrate losses. The use of high-resistivity silicon (HR-Si) substrate in Si-based RFICs has been proven to be a solution for reducing substrate losses, especially for suppressing substrate noise of the passive devices [1,2]. For the integration of CMOS devices with high-performance passive components for system-in-package (SiP) applications, the approach of integrated passive devices (IPDs) on surface-passivated HR-Si substrates can achieve good RF performances [3].

Surface channels build up at the silicon–dioxide/Si (SiO_2/Si) interface as a result of oxide contamination, interface states, or electrical biasing between a metal line above the field oxide and the Si substrate [4]. The surface channels result in the reduction of the effective substrate resistivity (ρ_{eff}) of the HR-Si substrate, hence, the transmission loss (α_{TL}) of on-chip transmission lines and passive devices on the SiO_2/HR-Si substrate increases due to induced substrate loss. Several surface-passivation techniques [2] have been used to reduce the substrate loss. One kind of common technique is inserting a polysilicon (poly-Si) surface-passivation layer (SPL) or more trap-rich SPLs such as amorphous silicon (α-Si) layer and RTA-crystallized Si layer between the SiO_2 and the HR-Si substrate.

Hot-wire chemical vapor deposition (HWCVD) can be used to deposit a quality-controlled nanocrystalline silicon (nc-Si) layer, which has successfully been used as a passivation layer and effectively suppresses transmission loss resulting from silicon substrate [2,5]. The substrate ρ_{eff} is up to 15 kΩ-cm at 20GHz [2]. In this work, we used one-turn inductors as test inductors to further characterize the surface-passivation capability for the SiO2/nc-Si-SPL/HR-Si substrates and estimate the feasibility of the high-performance integrated passive devices on the surface-passivated HR-Si substrates.

2. Experiments and Discussions

In this work, performances of square and octagonal spiral inductors on the nc-Si surface-passivated HR-Si substrates were studied. The octagonal spiral inductor has smaller edge field due to the smoother perimeter of metal trace, thus minimizing transmission loss resulting from penetration of edge field into substrate. Several one-turn inductors with different geometric parameters were designed, fabricated, tested, and compared.

The spiral inductors were fabricated on SiO2/nc-Si-SPL /p-type-HR-Si substrates. The resistivity of the HR-Si substrate is in the range of 1 to 5 kΩ-cm. The nc-Si SPL was deposited by HWCVD [2]. The oxide was deposited by plasma enhanced chemical vapor deposition (PECVD) and was 300 nm thick. 1.2-μm-thick Al layers were evaporated and patterned to form spiral patterns. The metal thickness is about half that of the top metal of commercial processes.

Fig.1 shows top-view photographs of one-turn octagonal and square spiral inductors. On-wafer S-parameter measurements were used for the extraction of inductor parameters including inductance and quality factor. After the parasitic de-embedding, the equivalent inductances and quality factors were extracted.

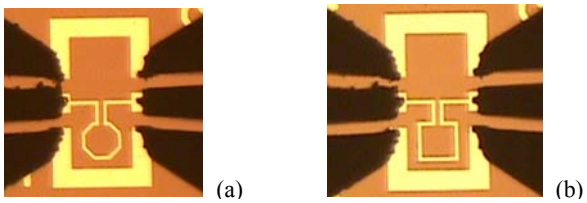

Fig. 1 Top-view photographs of one-turn (a)octagonal and (b) square spiral inductors.

Fig.2 shows quality factors of one-turn square inductors on the HR-Si substrates with and without an nc-Si SPL. For the purpose of performance comparison, spiral inductors on SiO_2/LPCVD-poly-Si-SPL/HR-Si substrates were also fabricated and measured. Both two SPLs are 100 nm thick. The metal width W and inner diameter d are 15μm and 80 μm respectively. Extracted inductances are about 0.43 nH. The one-turn inductor on the SiO_2-coated HR-Si substrates with an nc-Si SPL can give a higher Q value around 21.9 at 20 GHz. This is attributed to the higher substrate ρ_{eff}, which results in smaller substrate loss.

Fig. 3 shows inductances and quality factors of octagonal and square spiral inductors. The octagonal inductor has a higher quality factor and larger inductance due to its smoother perimeter and hence smaller edge-field loss resulting from penetration of edge field into substrate.

The inductance and quality factor of a spiral inductor depend on its inner diameter. Fig. 4 shows inductances and quality factors of the one-turn octagonal spiral inductors on

the SiO_2-coated HR-Si substrate with a 400-nm-thick nc-Si SPL. Three different diameter sizes, i.e. 80, 100 and 120 μm, were used. A set of extra inductances and quality factors of a foundry-provided inductor with 80-μm-thick inner diameter is also shown. In Fig. 4, the larger the inner diameter, the larger the inductance. The self-resonance frequency (SRF) of three inductors is higher than 20 GHz. For frequencies less than SRF, the larger the inner diameter, the larger the quality factor. The observed performances are similar to those of inductors provided by foundries, such as TSMC. It is also found that for the same inner diameter, the inductors on the SiO2/nc-Si-SPL/p-type-HR-Si substrates have larger inductances and larger quality factors at higher frequencies. The former is due to smaller cross-sectional area of metal trace. The latter is due to higher substrate ρ_{eff}, which is larger than 15 kΩ-cm at 20GHz [2].

There exist two independent loss mechanisms in inductors: the metal loss and the substrate loss [6]. At lower frequencies, the conduction loss of the metal layer, including skin and proximity effects, is the dominant Q-limiting mechanism. At even higher frequencies, the substrate loss sets the lower limit on the Q. Because the metal thickness of the designed inductors is about half that of inductors provided by foundries, the quality factors of the designed inductors at lower frequencies are slightly smaller due to larger conduction loss. As a whole, experimental results show that inductors on the the nc-Si passivated HR-Si can exhibit larger quality factors due to the good suppression effect of surface carrier channels of HR-Si substrates.

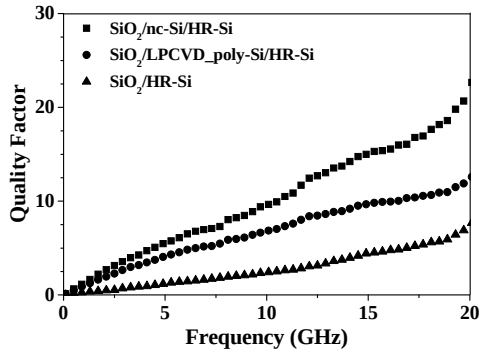

Fig.2 Quality factors of one-turn square inductors on the HR-Si substrates with and without a 100-nm-thick nc-Si SPL.

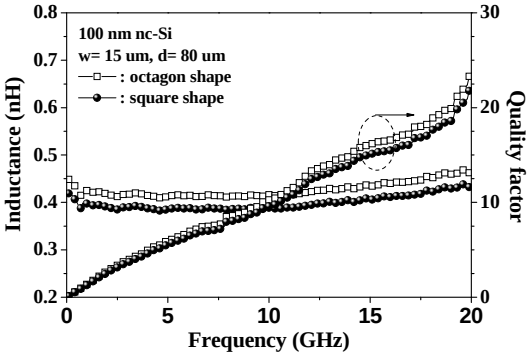

Fig.3 Inductances and quality factors for one-turn octagonal and square spiral inductors.

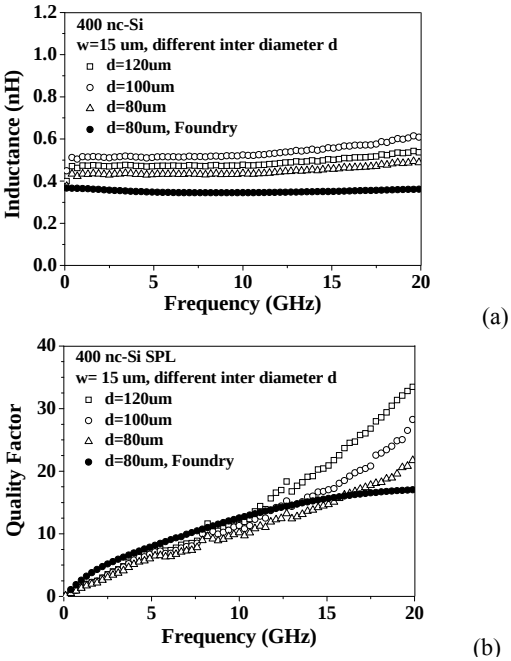

Fig. 4 (a)Inductances and (b)quality factors of the one-turn octagonal spiral inductors on SiO2/nc-Si-SPL / HR-Si substrates.

3. Conclusions

In this work, inductors on SiO2/nc-Si-SPL/HR-Si substrates are studied. For inductors with 80 μm diameter, the quality factor at 20 GHz is 21.9, 22.5, and 17 for the inductors on SiO2-coated HR-Si substrates with 100 nm and 400 nm nc-Si SPLs and a foundry-provided inductor, respectively. At higher frequencies, quality factors are higher due to suppressed substrate loss. For studied structures, the space between metal trace and substrate is less than 1 um and the thickness of metal trace is only 1.2 μm, hence the quality factors can be further enhanced by increasing thickness of oxide layer and metal trace.

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