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Fabrication of TiN/Si Contact with Low Electron Barrier Height and Electrical Characterization of Si-On-Insulator Using Back-Gate MOSFET

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1. Introduction

A Si-on-insulator (SOI) structure is beneficial to achieve high speed MOS devices because of the reduction of the parasitic capacitance. By virtue of the SOI structure and the high intrinsic carrier mobility, SiGe-on-insulator (SGOI) and Ge-on-insulator (GOI) are of great interest as a candidate substrate. However, the electrical characterization for the top semiconductor layer is not easy because the top layer is separated from a Si substrate by a buried oxide (BOX). A method for the characterization is the back-gate MOSFET, in which the BOX and bulk substrate are used as a gate insulator and a gate electrode, respectively [1].

There are two kinds of back-gate MOSFET structures. One is an accumulation mode, in which an Ohmic contact is used for source/drain (S/D). Another is an inversion mode, in which a rectified contact (junction) is used for S/D. By using these structures, bottom channel mobility can be simply evaluated. In addition, for the case of inversion mode, the ionized impurity concentration and the interface state density (D_{it}) between the semiconductor layer and BOX are also evaluated from threshold voltage and subthreshold slope (SS), respectively [2], although such evaluations cannot be done for the accumulation mode. Thus, the information obtained from the inversion MOSFET is much more than that from an accumulation MOSFET. The S/D in the inversion MOSFET should be fabricated using the metal/semiconductor contact at low temperatures, because the semiconductor layers such as SiGe and Ge are easily received the damage when the S/D was fabricated using impurity doping such as ion implantation and subsequent annealing or thermal diffusion at high temperatures.

Recently, we succeeded in the formation of a TiN/Ge contact with extremely low electron barrier height (Φ_{BN}) less than 0.1 eV, which was fabricated by direct sputter deposition from a TiN target and subsequent postmetallization annealing (PMA) at 350 °C [3]. Similarly, if a TiN/Si contact with low Φ_{BN} is formed using the same sputter deposition, the electrical characterization for $Si_{1-x}Ge_x$ layer ranging from x=0 to x=1 is made possible using inversion mode back-gate MOSFET.

In this study, we focus on the formation of TiN/Si contact with low Φ_{BN}. The contact prepared under optimal condition showed Φ_{BN} = 0.27 eV. We fabricated inversion-mode back-gate MOSFET using a TiN/Si contact and evaluated electron mobility. The obtained results are in good agreement with Si universal mobility. Thus, TiN/Si contact is useful for metal S/D in back gate MOSFET.

2. Experimental

The substrates were p-type and n-type (100) Si with a resistivity of 10 Ω·cm. A TiN film with a thickness of approximately 50 nm was deposited on the Si substrate by rf magnetron sputtering using a TiN target, which was similar to our previous work for Ge [3]. Then, a 50-nm-thick Al film was deposited by thermal evaporation, and the Al/TiN contact was patterned using a lift-off technique. Finally, PMA was carried out at a temperature of 400 °C in N_2 for 10 min, which was the optimal PMA condition.

Figure 1 shows the cross sectional image of Schottky back-gate n-MOSFET. A p-type SIMOX-SOI wafer with a diameter of 200 mm was used for a SOI back-gate MOSFET. Here, the thicknesses of SOI and BOX layers were 150 nm and 100 nm, respectively. The back-gate MOSFET was fabricated by forming the Al/TiN electrode (S/D) on a SOI layer and isolation etching of SOI layer.

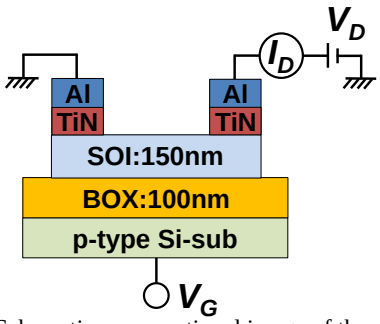

Fig. 1 Schematic cross sectional image of the fabricated Schottky back-gate n-MOSFET.

3. Result and Discussion

Figure 2 shows the *J-V* characteristics for the TiN/p-Si. The TiN/p-Si contact showed rectifying behavior with a high on/off ratio of 1.5×10^7. The hole barrier height of Φ_{BP} = 0.85 eV and an ideality factor of n = 1.17 were obtained from the forward *I-V* characteristic. Note that the Φ_{BP} found in this study is one of the highest barrier height among metal/p-Si contacts, which is comparable to that of an Er-Si/Si contact [4]. On the other hand, the TiN/n-Si contact showed Ohmic-like behavior at RT.

From our investigation of effective work function (Φ_m) using TiN-gate MOS capacitors, the Φ_m of TiN used in this study was 4.7 eV. The relation between Φ_{BN} and Φ_m for the metal/n-Si system is given by $\Phi_{BN} = 0.27\Phi_m - 0.52$ [5], which suggests Φ_{BN} = 0.75 eV and Φ_{BP} = 0.37 eV. However, the TiN/Si contacts indicated Φ_{BN} = 0.27 eV and Φ_{BP} = 0.85 eV, which implies that the charge neutral level and pinning

factor were modulated at the TiN/Si interface owing to the interlayer formation, just like a TiN/Ge contact [3].

In the case of a TiN/Ge contact, the interlayer causes the modulation of interface property. The interlayer was conductive according to the fact that the specific contact resistivity (ρ_C) was as low as $7.9\times10^{-6}\,\Omega\cdot cm^2$ [6]. To clarify the electrical property of the interface between TiN and Si, we measured the ρ_C of a TiN/n^+-Si contact using a circular transmission line model (CTLM) [7]. Here, the n^+ layer was formed by thermal diffusion of P at 1000 °C for 90 min and the carrier concentration was obtained as $3\times10^{20}\,cm^{-3}$ from Hall measurement. The CTLM resistance versus slit width (d) plots for a TiN/n^+-Si contact is shown in Fig. 3. The I-V characteristic for CTLM structure with d =14 μm is also shown in the inset in Fig. 3, confirming a good Ohmic characteristic. The ρ_C was estimated as $5.0\times10^{-5}\,\Omega\cdot cm^2$, which is more than 2 orders of magnitude lager than ρ_C of an Al/n^+-Si contact ($1.9\times10^{-7}\,\Omega\cdot cm^2$). By contrast, when an ultrathin SiO_2 less than 1 nm was inserted between TiN and Si as a tunnel barrier, the ρ_C was significantly increased up to $3\times10^{-3}\,\Omega\cdot cm^2$. Therefore, we speculate that the interlayer is a conductive layer or a very thin insulator with small band gap. Anyway, this small Φ_{BN} and ρ_C suggest that the TiN/Si contact is available to the Schottky S/D.

Figures 4 and 5 show the drain current (I_D) versus drain voltage (V_D) and gate voltage (V_G) characteristics for the fabricated back-gate MOSFET, respectively, indicating that channel conductions are well controlled by the V_G. The back-gate MOSFET exhibits well-behaved n-type inversion-mode operation, as shown in Fig. 4. Using the SS value of 203 mV/decade derived from Fig. 5, the D_{it} of the SOI/BOX interface was obtained as $1.1\times10^{11}\ cm^{-2}eV^{-1}$, which was a typical D_{it} value of SiO_2/Si [8]. The low field electron mobility (μ_0) was estimated from the slope of $I_D/g_m^{1/2}$-V_G plot, where g_m is the transconductance of the MOSFET [7]. The μ_0 was approximately 700 cm^2/Vs, which is almost the same as the universal electron mobility of Si. In another work, we have successfully demonstrated the device operation for Schottky n-MOSFET fabricated using TiN S/D in the Ge substrate [6]. Thus, the test samples for the electrical characterization of SOI, SGOI, and GOI substrates would be simply prepared in less damage.

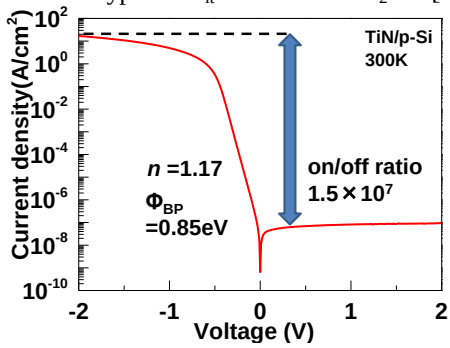

Fig. 2 J-V characterristics of TiN/p-Si contacts.

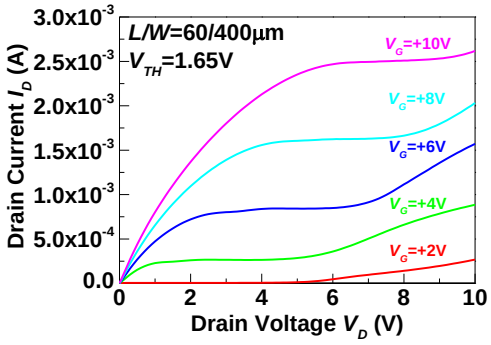

Fig. 4 I_D-V_D charactaristics of fabricated Schottky back-gate n-MOSFET.

4. Conclusion

We succeeded in the fabrication of a contact with low Φ_{BN} on Si by direct deposition of TiN. The ρ_C of a TiN/n^+-Si contact was as low as $5.0\times10^{-5}\,\Omega\cdot cm^2$, which ensured that the TiN/Si contact is available to S/D in Si Schottky n-MOSFET. We fabricated the back-gate Schottky MOSFET using the TiN/Si contact on a SOI substrate and demonstrated quite normal inversion-mode operation. Thus, electrical characterization for SOI, SGOI, and GOI substrates should be simple and accurate using the present TiN contact fabrication technique.

References

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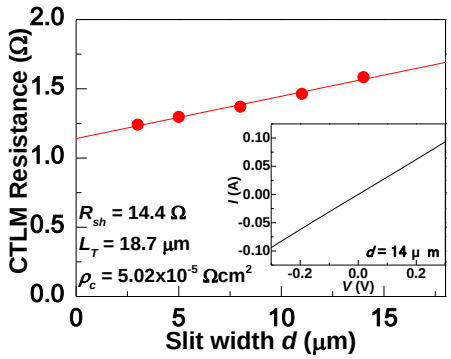

Fig. 3 The CTLM resistance versus slit width (d) plots for a TiN/n^+-Si contact and the current-voltage (I-V) characteristic for CTLM structure with d =14 μm.

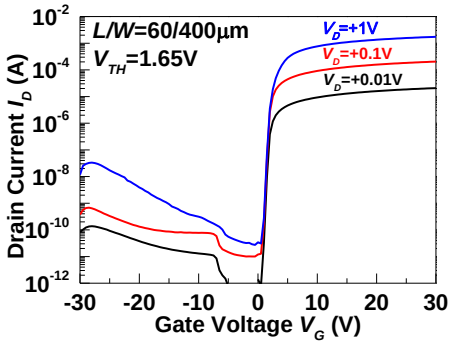

Fig. 5 I_D-V_G charactaristics of fabricated Schottky back-gate n-MOSFET.