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Grapho-Assembly Technology for Sub-Micron Accuracy 3D Chip Stacking with High-Density Through-Si Vias and Metal Microbumps

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1. Introduction

Three-dimensional (3D) chip stacking technologies can not only reduce the chip size but also dramatically increase signal processing speed and decrease power consumption without further scaling down device sizes [1]-[3]. Therefore, huge numbers of TSVs (through-silicon vias) formed in multiple stacked thin chips significantly shorten the lengths of global wires used in conventional system on a chip (SoC) and bonding wires used in system in packaging (SiP). Poly-Si-, W-, and Cu-TSVs have been mainly used in 3D LSI researches so far. In addition, Cu, Au, Cu-Sn, and Cu-SnAg have been employed as microbumps in 3D integration over the last decade. In recent years, 3D integration technology have been increasingly advanced in order for forming fine TSVs and metal microbumps, as shown in ITRS 2010 of Table 1. As shown in Fig. 1(a), we have reported W-TSVs with a diameter of 0.7 μm and a pitch of 3 μm [4]. On the other hand, 2-μm-square and 5-μm-pitch In-Au microbunps have been formed by evaporation and lift-off techniques as shown in Fig. 1(b) [5]. These fine TSV and microbump formation technologies require high-precision chip stacking. In other words, high alignment accuracies are essential for stacking high-performance LSI to give 3D chips. We have developed self-assembly technologies for high-precision 3D chip stacking [6]-[9]. In this study, we propose *Grapho-Assembly* to obtain sub-micron accuracy by combining with self-assembly using liquid surface tension.

2. Grapho-Assembly

"*Grapho*" means a *description* or *writing* in Greek. Derived from them, "*Grapho*" indicates artificial microstructure fabricated on substrate surface in semiconductor engineering. Grapho-epitaxy is well-known to be a crystal growth technique to integrate uniform crystallographic orientation on amorphous layers deposited on Si substrates on which Si micropatterns are regularly formed by lithography [10]. In order to three-dimensionally stack chips on chips or substrates in high alignment accuracy, we employ chips and substrates with various micropatterns formed by using standard photolithography and dry etching. We demonstrate that chips with micropatterns can be precisely self-assembled within 1 μm on chips/substrates with the corresponding micropatterns. In particular, we introduce micrometer-scale concavo-convex patterns formed on Si surface to *Grapho-Assembly* with water droplets.

3. Fabrication of Chips with Concavo/Convex Micropatterns

The concavo-convex micropatterns on bare Si wafers were formed by deep reactive ion etching using Bosch process with SF_6 and C_4F_8 gases. Figure 2 shows the cross-sectional structure of the resulting top chips A having three types of convex slit micropatterns with widths of 10, 20, 50 μm on chip surface. The corresponding bottom chips A have concave micropatterns with widths of 12, 26, 70 μm. Any chips have 42-μm-height/depth slit microstructures. In addition, top chips B and bottom chips B with octagonal-prism microstructures were fabricated and used for Grapho-Assembly experiments, as shown in Fig. 3. The height/depth of the microstructures was controlled and differentiated by using oxide etching selectivity to the Bosch process, as shown in Fig. 4. The resulting height differences were 11, 24, and 42 μm. Finally, these wafers were diced to give the two types of Si chips: top chips A/B with convex micropatterns and bottom chips A/B with concave ones.

Self-assembly procedure is described in our previously papers [6]-[9]. Here, we used ultrapure water as liquid for self-assembly. First, a 1- or 2-μl droplet of water was supplied on bottom chips with concave micropatterns. Then, top chips with convex micropatterns were dropped on the bottom chips. Immediately after chip release, the top chips were aligned to the bottom chips. After that, it took several minutes to completely evaporate the water droplets at room temperature. The alignment processes were observed with a digital microscope (VHX-900SP, Keyence).

4. Evaluation of Alignment Accuracy

Figure 5 shows self-assembly processes after releasing top chip A with 10, 20, 50-μm-width convex slit micropatterns to the corresponding bottom chip A with 12, 26, 70-μm-width concave ones. The water droplet was fully evaporated in 10 minutes at room temperature. Finally, the top chip was precisely assembled on the bottom chip A, and consequently, the convex micriopatterns perfectly fit in the concave micropatterns after mechanical compression. The alignment accuracy is estimated to be within 1 μm.

On the other hand, another top chip B with 10, 20, 50-μm-diameter convex octagonal-prism microstructures was self-assembled to the corresponding bottom chip B with the concave microstructures. The top chip was precisely self-assembled to the bottom chip B. Figure 6 shows IR images of the surface of the octagonal-prism microstructure formed on the top chip B self-assembled onto the other bottom chip B with concave microstructure. The top chip B with the convex microstructure was successfully fitted into the concave ones. The accuracy is also estimated to be within 1 μm.

Conclusions

We have proposed and developed Grapho-Assembly to realize high-precision 3D chip stacking. Chips withconvex micropatterns are precisely self-assembled on the other chips with cancave ones. The resulting alignment accuracy (< 1 μm)was very high enough to stack LSI chip with fine-pitch TSVs and microbumps.

Acknowledgements

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Table 1 Intermediate interconnect level TSV roadmap reported in ITRS 2010.

Intermediate Level, W2W 3D-stacking	*2009-2012*	*2013-2015*
Minimum TSV diameter	1-2 μm	0.8-1.5μm
Minimum TSV pitch	2-4 μm	1.6-3.0 μm
Minimum TSV depth	6-10 μm	6-10 μm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0-1.5 μm	0.5-1.0 μm
Minimum contact pitch	2-3 μm	2-3 μm
Number of tiers	2-3	8-16 (DRAM)

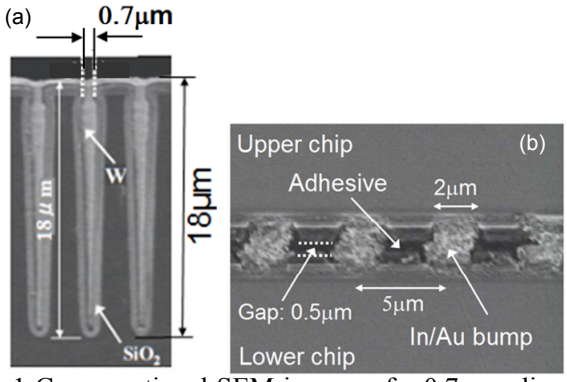

Fig. 1 Cross-sectional SEM images of a 0.7-μm-diamter W-TSV and a 5-μm-pitch In-Au microbump daisy chain.

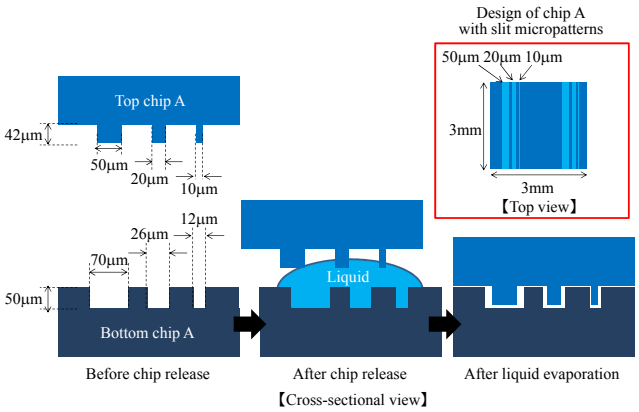

Fig. 2 Structure and design of top and bottom chips A with slit micropatterns, and their self-assembly flow.

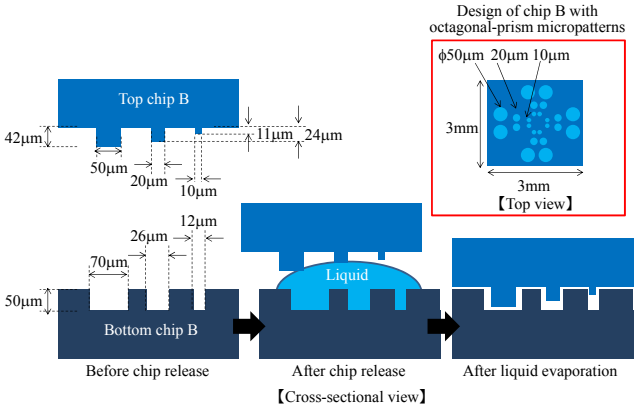

Fig. 3 Structure and design of top and bottom chips B with octagonal-prism microstructures, and their self-assembly flow.

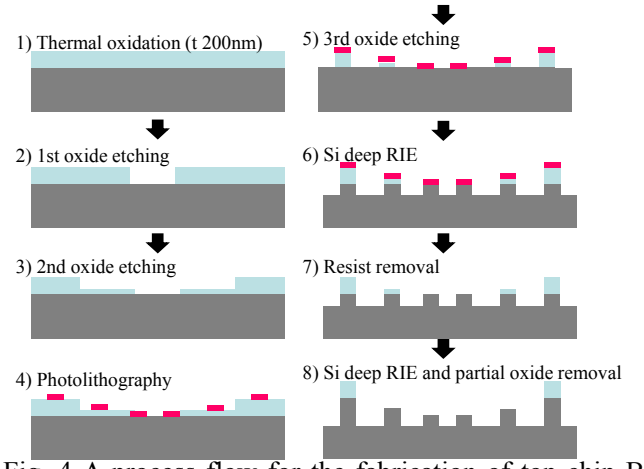

Fig. 4 A process flow for the fabrication of top chip B with convex octagonal-prism micropatterns.

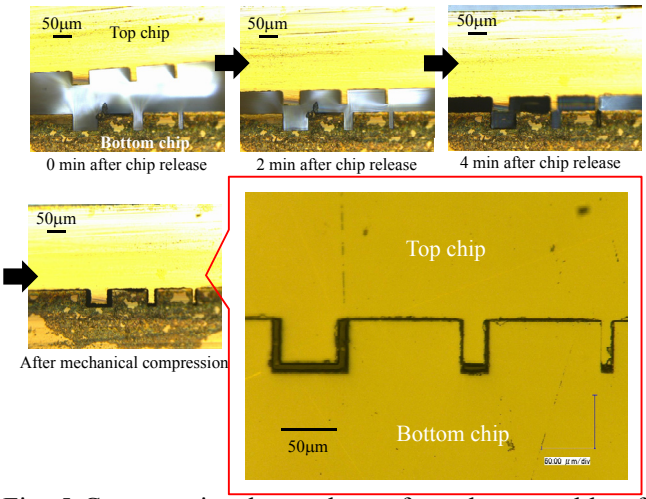

Fig. 5 Cross-sectional snapshots of grapho-assembly of chips A with slit micropatterns.

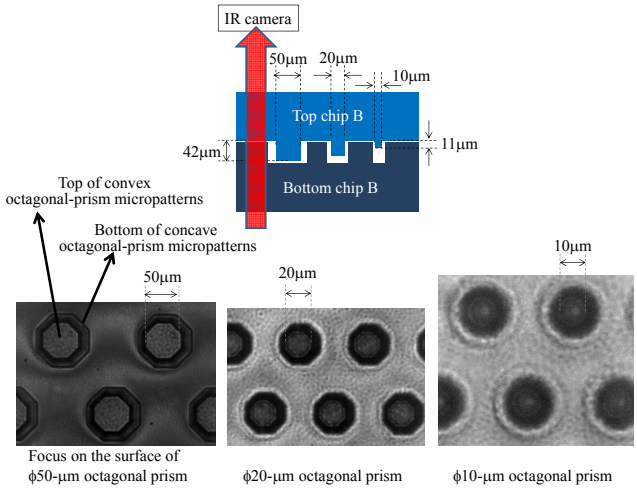

Fig. 6 IR images of the surface of the octagonal-prism microstructurse formed on a top chip B self-assembled onto another bottom chip B with concave microstructures.