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The Influence of Cu Diffusion from Cu Through-Silicon Via(TSV) on Device Reliability in the 3D LSI by Using *C–V* and *C–t* Measurements

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1. Introduction

Demands for the high-performance, high-speed, and highly integrated systems have been significantly increased for the future ubiquitous society. To suffice the requirements, many researchers and product vendors recently present three-dimensional (3D) LSI technologies that can stack various kinds of functional blocks such as processor, memory, sensor, logic, analog and power ICs into one stacked chip [1].

To accomplish a compact size 3D LSI, each functional wafer should be thinned down below 30 μm and connected by high dense Cu TSVs and metal micro-bumps. However, this may cause severe degradation of device reliability in the 3D LSI as shown in Fig. 1. The mechanical strain/stress and crystal defects in a thinned wafer [1] and easy metal contamination from the wafer backside [2-3] induced by the wafer thinning, and local mechanical strain/stress induced by Cu TSV is hot issues for the device reliability of 3D LSI. Furthermore, Cu diffusion from Cu TSV and metal contamination from backside of wafer is another concern for achieving high reliable 3D LSI. Cu TSV is most commonly achieved by silicon deep etching, oxide liner deposition and sputtering with barrier and seed layers in the TSV which is followed by Cu electroplating before the back end of line (BEOL) process. However, when the blocking property of the barrier layer to Cu is not sufficient, Cu atoms may rapidly diffuse to active region from Cu TSV and cause the electrical characteristic degradation after conventional post-BEOL H_2 sintering anneal process for 30 min at 400 ^{o}C. To avoid Cu contamination issues from a backside of the thinned wafer [3-4] and Cu TSV and to achieve high-end 3D LSI, we developed low-temperature and fine-size backside Cu TSV formation technology.

In this paper, we have investigated Cu gate electrode MOS capacitor with Cu TSVs fabricated on thinned wafer by *C-V* and *C-t* method and evaluated the Cu contamination from the Cu TSVs and from the backside of wafer. Furthermore, the degradation of TSV oxide with barrier layer is also evaluated using *C–V* and *C–t* measurements performed before and after annealing, various annealing time and temperatures.

2. Experimental

To electrically characterize the Cu diffusion behavior from Cu TSV and backside of metal contamination, the Cu/Ta gate electrode MOS capacitor with Cu TSVs was fabricated. 280 μm thick P-type silicon wafers with substrate resistivity of 10 ～ 15 Ω·cm were used. After the formation of 50 nm screen oxide, wafer thinning process was performed below 100 μm thickness of wafer by grinding and CMP process. And TSV formation was performed by silicon deep etching with P.R. mask. TSV etch is subsequently followed by the formation of a 100 nm thick oxide liner into via hole and formation of Ta barrier layers with thicknesses of 100 nm as shown in Fig 2-a). The minimal thicknesses of Ta layers in TSVs are approximately 30 nm (100 nm at the surface) as shown in Fig. 2-b). A 200 nm thick Cu seed deposition is then carried out before the subsequent filling of TSVs with electroplated Cu. A 4 μm thick Cu layer acts as both gate electrode and TSV conductor. The metal gate electrode composed of Cu and Ta layers was patterned into 1000 μm square size to form the trench MOS capacitor including 50×50 trenches array. Finally, to evaluate the backside contamination, a 50 nm-thick Cu was evaporated on the back side of the thinned wafers to introduce a metallic impurity into the silicon substrate. The process flows for the fabrication of MOS capacitor with Cu TSVs on the 100 μm-thick silicon wafers are shown in Figure 3.

To intentionally diffuse Cu atoms from Cu TSV and backside of wafer into the silicon substrate, the wafers were annealed at 300 ºC and 400 ºC in N_2 ambient for various annealing times, respectively. Each measurement of *C-V* and *C-t* was performed using Agilent B1500A with 1MHz oscillation signal at 10 mV.

3. Results and discussion

Figure 4 show the *C-V* and *C-t* curves of the Cu/Ta gate electrode MOS capacitor without Cu-TSVs. At 300 ºC annealing for various annealing time, even though the flat-band voltage in *C-V* curves, as shown in Fig. 4(a), does not change, but *C-t* curves of the MOS capacitor, as shown in Fig 4(b), show a severe degradation with a short recombination time as compared with initial recombination time. It means that the protection of Ta layer against Cu diffusion from gate electrode is well performed. On the other hands, it is found that the Cu contamination is obviously induced by the backside Cu diffusion at 300 ^{o}C. Figure 5 show the *C-V* and *C-t* curves of MOS capacitor with the annealing temperature at 400 ºC for various annealing time. *C-V* and *C-t* curves of the MOS capacitor show a severe degradation with a flat-band voltage shift and short recombination time as compared with those of initial states. It means that the Cu contamination in the active region is induced by Cu diffusion both from the backside and the Cu/Ta gate electrode. With same method, *C-V* and *C-t* curves of a Cu/Ta gate electrode MOS capacitor with Cu TSVs were measured with different annealing temperature as shown in Fig. 6 and Fig. 7, respectively. Resemble results of *C-V* and *C-t* curves for a Cu TSVs MOS capacitor with increasing annealing time as compared with those of MOS capacitor without TSVs was achieved. However, the contamination of active region in MOS capacitor with Cu TSVs is more seriously degraded as compared with those of MOS capacitor without Cu TSVs. It means that Cu atoms diffuse into the active region from the Cu TSV due to the poor coverage of Ta layer and reach to the Si-SiO_2 interface of the active region and consequently the generation lifetime is significantly reduced during the annealing at 400 ºC.

Conclusions

The influence of Cu contamination from the Cu TSV was electrically characterized by *C-V* and *C-t* analysis using Cu/Ta

gate electrode MOS capacitor with and without Cu TSVs. It revealed that Cu atoms diffuse easily into the active region from Cu TSV and backside Cu contamination even with thick Ta barrier layer and thick silicon thickness after post-BEOL H_2 sintering anneal at 400 ºC. We successfully developed a low-temperature and fine size backside Cu TSV formation technology to avoid Cu contamination issue and to achieve high reliable and high-end 3D LSI.

Acknowledgements

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References

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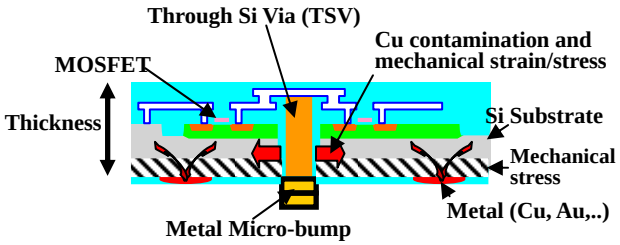

Fig. 1 The influence of mechanical stress and metal contamination on device reliability in 3D LSI.

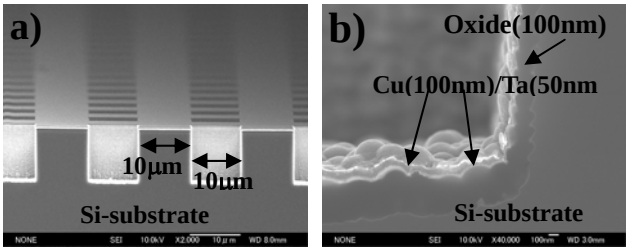

Fig. 2 FE-SEM images of a sample with TSVs deposited oxide, Ta and Cu seed layer: a) low angle image and b) cross-sectional image of bottom area TSV.

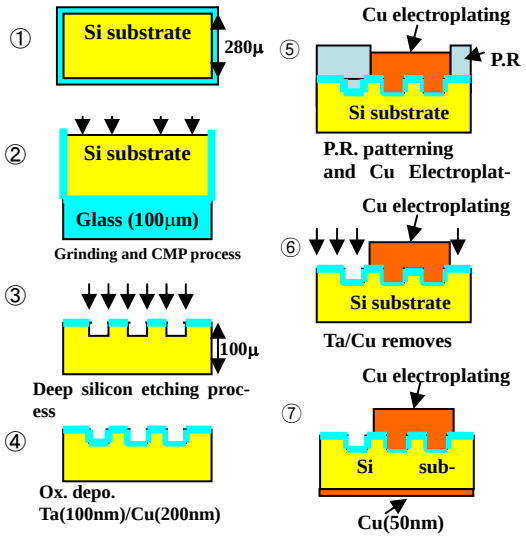

Fig.3 Process flow for the fabrication of MOS capacitors with Cu TSVs on 100 μm-thick silicon wafers.

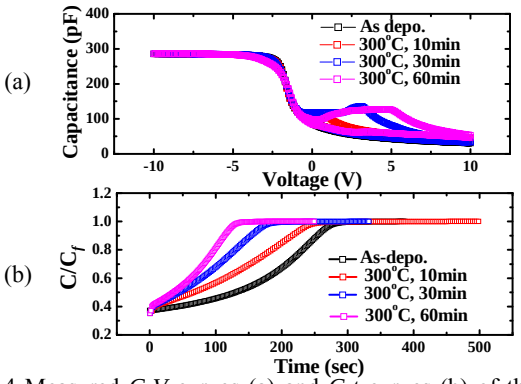

Fig. 4 Measured *C-V* curves (a) and *C-t* curves (b) of the MOS capacitor without Cu TSV annealed at 300 °C for a various annealing time, respectively.

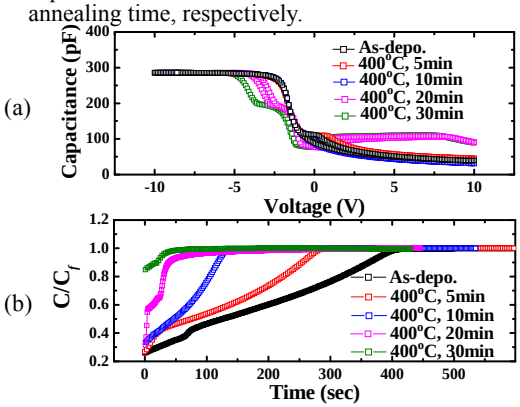

Fig. 5 Measured *C-V* curves (a) and *C-t* curves (b) of the MOS capacitor without Cu TSVs annealed at 400 °C for a various annealing time, respectively.

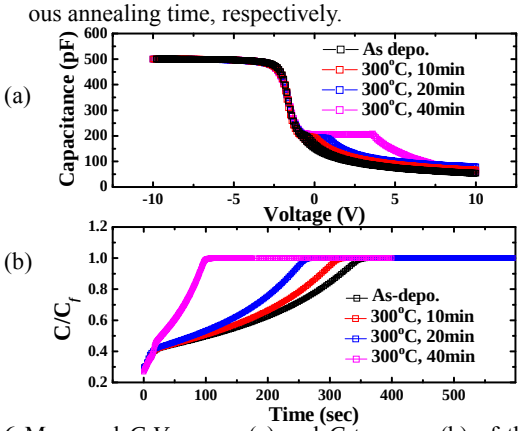

Fig. 6 Measured *C-V* curves (a) and *C-t* curves (b) of the MOS capacitor with Cu TSVs annealed at 300 °C for a various annealing time, respectively.

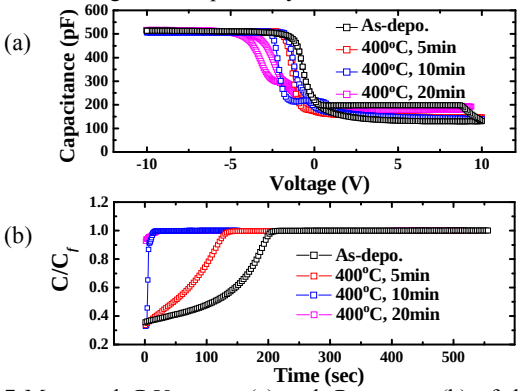

Fig. 7 Measured *C-V* curves (a) and *C-t* curves (b) of the MOS capacitor with Cu TSVs annealed at 400 °C for a various annealing time, respectively.